Dynamic X-ray Flat Panel Detector with High Imaging Quality Based on Amorphous Silicon PIN Photodiode

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Abstract

X-ray flat panel detectors based on TFT are widely used in the fields of medical digital imaging and industrial inspection. This paper is based on the a-Si TFT+PIN detection panels. Dynamic detection is achieved by high thickness PIN, and low noise is realized simultaneously. On this basis, we start from the principle of lag generation and design new pixel structure and process. Ultimately, dynamic detection with low lag is achieved.

Author Keywords

X-ray flat panel detector; thin film transistor; PIN photodiode; dynamic detection; lag; noise.

1. Introduction

Digital radiography (DR) is an important technology in today's medical imaging diagnosis, where the x-ray flat panel detector, as a photoelectric conversion component, is a key part of it. The detector technologies that have been widely commercialized include: a-Si indirect type, a-IGZO indirect type, a-Se direct type, and CMOS indirect type. Generally, among the aforementioned indirect flat panel detectors, the a-Si PIN photodiode is usually chosen as the photoelectric conversion device due to its high quantum efficiency in the range of the visible to near-infrared light, mature process, low cost, and high yield.

With the development of digital radiology, x-ray flat panel detector technology is also constantly advancing and breaking through. In recent years, flat panel detectors have expanded from the field of medical digital imaging to industrial inspection [1][2]. In the aforementioned application fields, there is a common demand for higher technical requirements for x-ray flat panel detectors, namely high-frequency dynamic detection, which can obtain high-quality image information of the detected object continuously and smoothly[5][6].

This paper designs and manufactures a dynamic x-ray flat panel detector which detection frequency is higher than 30fps, and based on this detector, the dynamic imaging quality is studied. The thickness of the a-Si PIN Photodiode is increased by 30%, which can increase the maximum frame rate by 30%. While achieving high-frequency acquisition, the thermal noise of the photodiode is reduced by 12%, and the total output noise of the detector is reduced by 5%, thereby improving the SNR of the detector. On this basis, in response to the deterioration on lag caused by the increased thickness of PIN, various thin-film deposition processes and dry etching processes to reduce PIN defects have been explored. In summary, high-quality dynamic x-ray image acquisition has been achieved.

2. Discussions

Theory: Usually, for an image acquisition system, increasing the rate of image acquisition will inevitably decay the image quality. Therefore, it is necessary to employ certain methods to maintain a high level of image quality while enhancing the frequency of image acquisition. In this context, for medical digital imaging and industrial inspection, image quality is typically assessed through signal-to-noise ratio (SNR) and lag.

The necessary condition for achieving high-frequency dynamic acquisition is to reduce the row scanning time of the detector. Commonly, during detector design, the Conventional method is to decrease the RC delay of the pixel in the detector's acquisition array (where R is the on-resistance of the TFT, R_{on}, and C is the storage capacitance of the photodiode in the pixel, C_{pd}). On one hand, if an attempt is made to reduce R_{on}, it will inevitably increase the W/L of the TFT channel, thereby decreasing the area of the photodiode in the pixel and consequently reducing the acquired signal. Moreover, the enlargement of the TFT also brings greater shot noise from the TFT, which in turn lowers the SNR. On the other hand, if an attempt is made to reduce C_{pd}, it is possible to decrease C_{pd} without changing the area of the photodiode by increasing the thickness of the PIN. This method not only maintains the level of the signal but also reduces the shot noise and thermal noise of the PIN, thereby achieving an enhancement in SNR. Additionally, the requirement for high-frequency dynamic acquisition is achieved through the reduction of pixel RC.

On the basis of achieving dynamic acquisition and maintaining a high level of SNR, we also need to pay attention to another important indicator of image quality, namely lag. The occurrence of lag is usually caused by the photo-generated carriers trapped into defects in the PIN photodiode. Therefore, for the aforementioned scheme of achieving dynamic acquisition and high SNR by increasing the thickness of the PIN, it is actually unfavorable for achieving a low level of lag [3][4]. This is because, under the premise of keeping the projection area of the PIN unchanged, increasing the thickness of the PIN means an enlargement in the volume and surface area of the PIN a-Si material. When the bulk defect density and surface defect density of the PIN a-Si material are kept constant, the total number of bulk defects and the total number of sidewall surface defects increase. As a result, during the photoelectric conversion, more defects will trap more photo-generated carriers, thereby leading to a more pronounced lag phenomenon. To overcome this disadvantage, it is necessary to develop PIN thin-film deposition processes and etching processes with low defect density.

Detector Fabrication: The research in this paper is based on a 21cm×21cm x-ray flat panel detector made on an a-Si TFT G5 production line, with a pixel size of 200μm×200μm. The pixel circuit structure is PPS (passive pixel sensor) type, consisting of one switching TFT used for reading， and one a-Si PIN photodiode. Figure 1 shows the schematic diagrams of the detector module structure, the top view structure and the cross section of the pixel. Combining the principles above, it can also be clearly seen from the figure below that the areas of the TFT and the PIN photodiode in the pixel are interdependent. Therefore, increasing the detector's dynamic acquisition frame rate by enlarging the TFT W/L will have a negative impact on the PIN.

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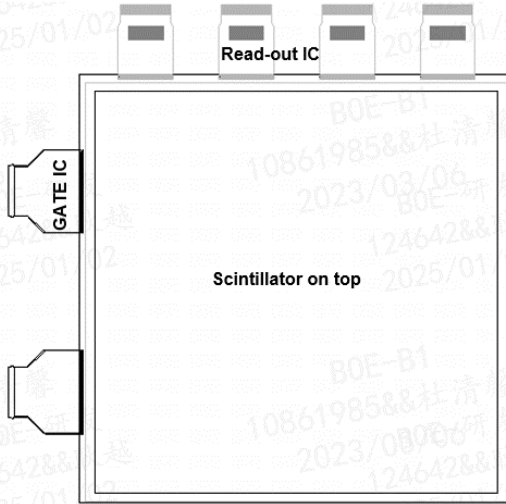
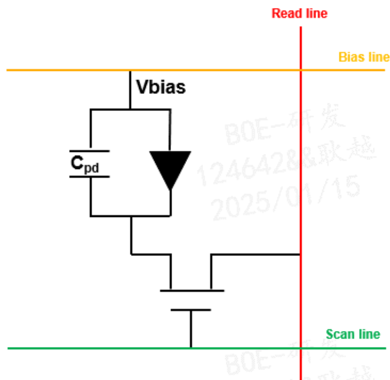
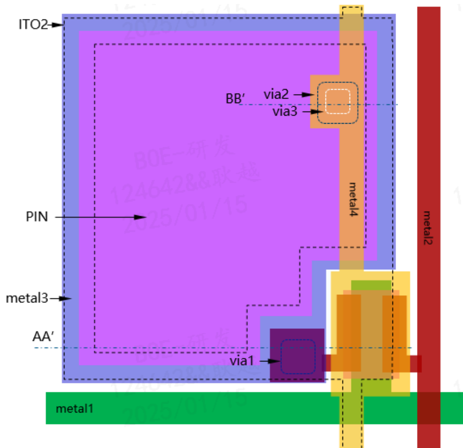
After the completion of the detector panel fabrication, it is necessary to bond the scanning IC and the signal reading-out IC to achieve the image acquisition function. At the same time, a scintillator layer needs to be made above the pixels in the acquisition area of the detector panel, which is used to convert x-ray into visible and near-infrared light that can be detected by the a-Si PIN.



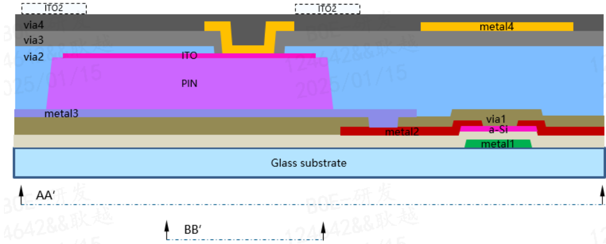
(a) Schematic diagram of the detector module structure



(b) Schematic diagram of the detector pixel circuit



(c) Schematic diagram of the top view structure of the detector pixel



(d) Schematic diagram of the cross section of the detector pixel

Figure 1. Schematic diagrams of the detector module structure, detector pixel circuit, the top view structure and the cross section of the detector pixel.

Discussions: Firstly, through theoretical calculations, the research analyzed the changes in the theoretical maximum dynamic acquisition frame rate that the 21cm×21cm flat panel detector used in this study can support under different PIN photodiode thicknesses, as well as the corresponding changes in photodiode thermal noise, shot noise, and the total output noise of the detector. This was done to illustrate the impact of increasing PIN thickness on the detector's dynamic acquisition frame rate and SNR. Subsequently, based on this analysis, the paper explored some methods to reduce the defects in the a-Si PIN film layer, in order to overcome the deterioration on lag caused by the increased PIN thickness.

(a) The Dynamic Acquisition Frame Rate and Noise

The table below calculates the theoretical maximum acquisition frame rate and noise changes of the 200μm×200μm pixel in a 21cm×21cm flat panel detector at different PIN thicknesses. It can be seen that increasing the PIN thickness can significantly improve the maximum acquisition frame rate, indicating that enhancing the dynamic acquisition capability of the detector by increasing the PIN thickness is highly effective. Additionally, the increase in PIN thickness also significantly reduces the detector's noise. On one hand, the increased PIN thickness reduces the electric field strength of the PIN storage capacitance C_{pd}, leading to a decrease in PIN dark leakage, and consequently, a reduction in the PIN shot noise $\sigma_{shot} = \sqrt{I_{PIN-leakage} \cdot t_{integration}/q}$. On the other hand, the increased PIN thickness reduces the capacitance C_{pd} of the PIN storage capacitance, thereby decreasing the PIN thermal noise $\sigma_{KTC} = \sqrt{2kt \cdot C_{PD}/q}$. Overall, the increase in PIN thickness optimizes the system's total output noise.

Table 1. The variation of PIN storage capacitance, maximum acquisition frame rate, and noise with the deposition thickness of PIN

PIN thickness (μm)	PIN storage capacitance (pF)	Max. fps (frame/s)	PIN shot noise (e-)	PIN thermal noise (e-)	Total output noise (e-)
0.7	4.83	17	89.5	1248.3	1754.5
0.9	3.70	22	78.4	1092.6	1646.7
1.2	2.75	30	67.5	941.9	1550.4
1.5	2.18	38	60.2	838.7	1489.6

Further, through simulation analysis of the detector's ability to read the photoelectric conversion signal accumulated in the capacitance C_{pd} formed by the PIN during high-frequency dynamic acquisition, that is, the integrity of the detector's signal reading current's integration of photo-generated carriers. Taking the case of a 1.2μm thick PIN as an example, Figure 2 shows the simulation results indicating that, considering the RC loading of the scan line, the completeness of signal

acquisition can reach 99.9%, which demonstrates that the detector can fully support the high-frequency dynamic acquisition of 30fps.

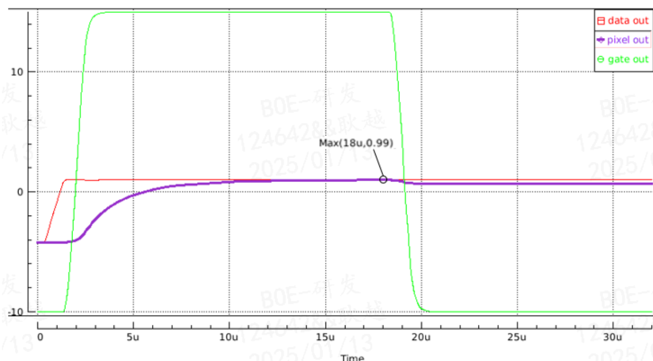


Figure 2. The detector's ability to read the accumulated charge in the capacitance C_{pd} formed by the PIN during dynamic acquisition at 30fps.

(b)Lag Optimization

Based on the analysis of the theoretical calculation results mentioned above, increasing the thickness of the PIN can improve the maximum acquisition frame rate of the x-ray flat panel detector and can also significantly reduce the detector's noise. Taking this solution as a foundation, by exploring methods to optimize the detector's lag, the ultimate goal of high-quality dynamic x-ray image acquisition can be achieved. Starting from the principle of lag generation, we designed new pixel structure and process schemes to reduce the defect density of a-Si PIN or to accelerate the release of carriers captured by PIN defects. Then we evaluated the level of lag through real product fabrication and image acquisition.

The testing method for lag is as follows: First, before the exposure action begins, take multiple dark images before exposure and select the last few dark images with relatively stable gray level. Take their average value as the dark base template. Next, start the exposure and continue for multiple frames to allow the defects in the PIN a-Si to combine with the photo-generated carriers, causing carrier trapping, and record the exposure image of the last frame. Then, terminate the x-ray source to put the detector system back into the dark state. In this stage of the dark state, although the external light source conditions are the same as before exposure, the PIN in the detector pixel has accumulated a certain number of carriers trapped by the PIN a-Si. Therefore, there is a difference between the dark images collected in this stage and before exposure. The ratio of this difference to the total amount of the sampled photo-generated carriers is the lag.

It should be noted that this paper only presents an example of lag testing and calculation. In reality, different detector manufacturers may have certain differences in their evaluation methods for lag, mainly in the number of images collected at each stage and the frequency of image acquisition. Additionally, for various categories of detector products, the lag after different numbers of exposure frames are also evaluated, the common examples including the 1st frame lag after exposure, the 2nd frame lag after exposure, and the 5th frame lag after exposure. Although there are the aforementioned differences, all manufacturers are completely consistent in the principles of lag testing and calculation. Therefore, the testing methods do not affect the determination of the detector's lag level. In this paper, the 5th frame lag after exposure is used as a unified standard.

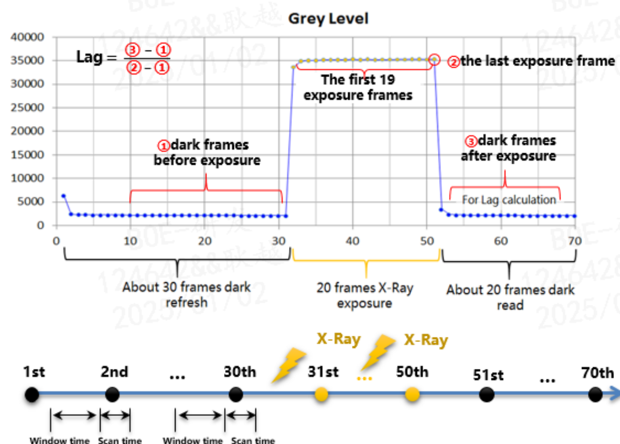


Figure 3. The testing principle of detector's lag.

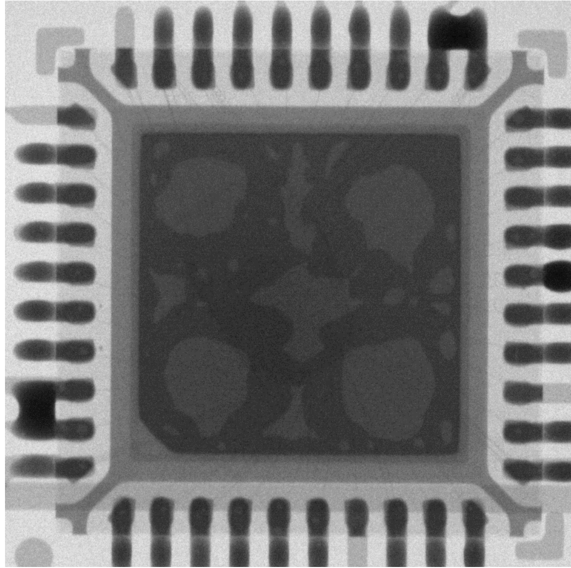
The following presents some research results on optimizing lag.

1. Pixel Structure: As shown in the top view and cross-sectional schematic diagrams of the pixel in Figure 1, a ring-shaped conductive material structure is designed to promote the release of carriers captured by a-Si defects in the PIN. The design principle is as follows: During the dry etching process of the PIN, a large area of sidewall profile is formed, which usually accumulates a large number of sidewall defects. This ring-shaped conductive structure can completely cover the PIN sidewall slope in the top view and is connected to the bias line in the peripheral circuit, also serving as the reference voltage for the reverse bias of the PIN. Under the action of this structure, the photo-generated carriers captured by the PIN sidewall defects will be accelerated to release, thereby reducing lag. In addition, it should be noted that the thin film material used to make this ring-shaped conductive structure in this paper is ITO, with the aim of optimizing lag without reducing the fill factor of the pixel.
2. PIN Deposition Process: The temperature during the deposition of the i-layer (intrinsic layer) of the PIN. Theoretically, a higher deposition temperature is more conducive to forming a PIN a-Si film layer with a lower bulk defect density. This is because, during the formation of amorphous Si thin films, there are a certain number of film defects, including dangling bonds, vacancies, and weak Si-Si bonds, among which the weak Si-Si bonds are prone to breaking and forming Si dangling bond defects. Raising the deposition temperature of a-Si can reduce the number of weak Si-Si bonds, thereby reducing the defect density of the PIN a-Si material, and consequently reducing lag.
3. PIN Dry Etching Process: PIN dry etching power. Theoretically, a lower etching power is more conducive to forming a PIN a-Si film layer with a lower sidewall defect density. This is because the PIN, as a photoelectric conversion layer, is usually quite thick. During the PIN dry etching process, a large sidewall area is formed. The higher the etching power, the greater the degree of damage to the sidewall, leading to more sidewall defects. By reducing the dry etching power, the sidewall defect density of the PIN a-Si material can be lowered, thereby reducing lag.

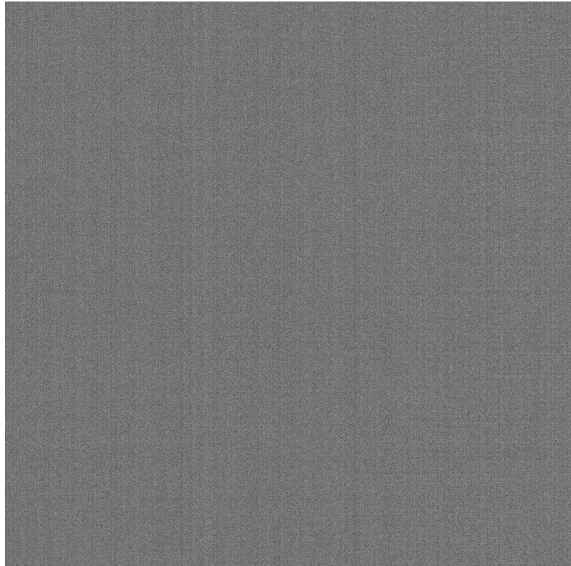
3. Summary

We designed and fabricated a 21cm×21cm flat panel detector with a pixel size of 200μm×200μm. To meet the requirements for high-frame-rate dynamic acquisition, this was achieved by fabricating PIN devices with a thickness of 1.2 to 1.5um, and simultaneously, a lower noise level was realized, thereby achieving a higher SNR (Signal-to-Noise Ratio) level. On this basis, to address the negative impact of increased lag due to the high thickness of PIN, we started from the principle of lag generation and designed new pixel structure and

process schemes. Through real product fabrication and image acquisition, we evaluated the level of lag. Finally, based on the research results of this paper, the flat panel detector can support dynamic acquisition at 30fps, and the 5th frame lag after exposure is only about 0.2%. Figure 6 shows the 20th exposure frame and the 5th dark frame after exposure of the detector. It can be seen that the impact of lag is hardly detectable in the 5th dark frame after exposure.



(a) The 20th exposure frame



(b) The 5th dark frame after exposure

Figure 6. The 20th exposure frame and the 5th dark frame after exposure of the 21cm×21cm detector.

4. References

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