MicroLED Pixel Circuit with A Novel NMOS-Oxide TFT Inverter for Reducing Falling Time and Enhancing Gray-Level Expression

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Abstract
In this paper, we propose a new circuit that significantly reduces the falling time by adopting a novel oxide thin-film transistor (TFT)-based inverter for pulse width modulation (PWM). Compared to existing n-channel metal-oxide-semiconductor (NMOS)-only pixel circuits that rely solely on the SWEEP signal, the falling time is significantly reduced to 0.125 μs, enabling the expression of up to 25 gray levels without wavelength shift or pulse distortion.

Author Keywords
Micro-light-emitting diode (μLED); Oxide thin-film transistor (TFT); Inverter; Pixel circuit; NMOS; Falling time

1. Introduction
Micro light-emitting diodes (μLEDs) have attracted interest in the display industry for their advantages, such as low power usage, high thermal stability, resistance to burn-in, and surpassing OLEDs in these areas [1]-[2]. Gray levels in μLED displays are controlled using pulse width modulation (PWM), which adjusts the emission time through a sweep signal while maintaining a constant current [3]-[4]. In an ideal case, the voltage input to the gate of the constant current generation (CCG) transistor changes, and then the CCG transistor transits from the on to the off state. However, when a sweep signal is used as the input, the slope at the transition point is low, resulting in an extended falling time. At low gray levels, where the pulse widths become shorter than the falling time, this leads to reduced peak current and potential color distortion [5]-[7]. Therefore, an inverter structure has been introduced recently to reduce the falling time [8]-[10].

Figure 1 shows how PWM operation is implemented using an inverter-based circuit structure. In an inverter-based pixel circuit, the CCG transistor is controlled using the output signal of the inverter. In this case, the slope at the transition point is steep, reducing the falling time of the μLED current. However, conventional inverter circuits use complementary metal-oxide-semiconductor (CMOS) transistors, which require a p-channel metal-oxide-semiconductor (PMOS) pull-up transistor, making it challenging to fabricate the pixel circuit solely with n-type oxide thin-film transistors (TFTs). Therefore, an inverter design using only n-channel metal-oxide-semiconductor (NMOS) is required. This approach was first addressed in the gate in panel (GIP) circuit and integrated circuit (IC), which include the NMOS-only basic inverter that employs a diode-connection structure in the pull-up stage [11], zero-V_{GS} inverter [12]-[13], and bootstrapping (pseudo-E) inverter [14]-[16]. However, the NMOS inverter with a basic diode-connection structure has limitations, such as low inverter gain and limited output swing [17]. By contrast, the zero-V_{GS} inverter performs well in depletion-mode operation but suffers significant degradation during the transition to enhancement mode due to the threshold voltage (V_{TH}) shifts, which makes it susceptible to variations. Thus, the bootstrapping structure-based inverter is noted for its high gain and V_{TH} shift stability.

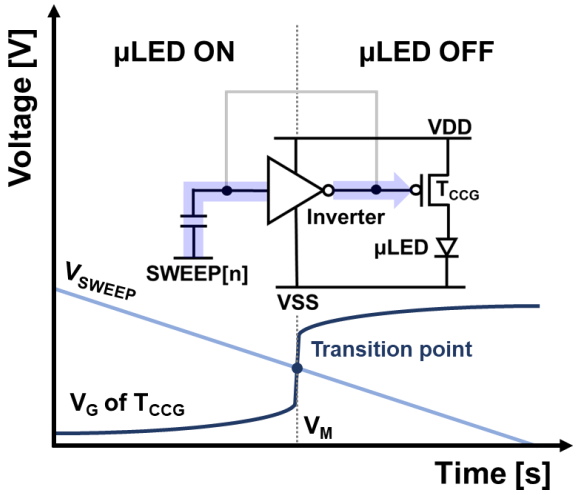
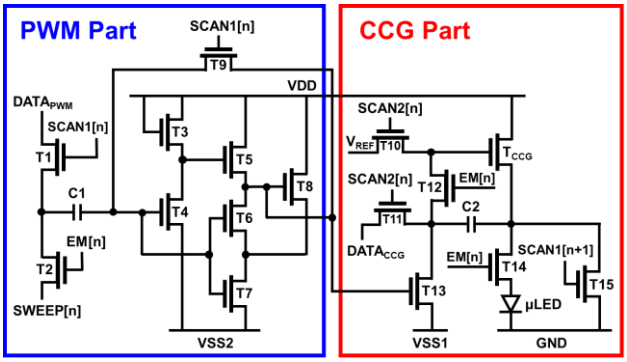
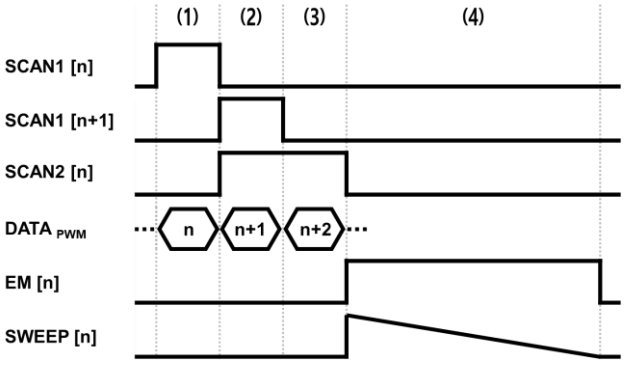


Figure 1. PWM operation of the μLED pixel circuit using an inverter-based structure.



(a)



(b)

Figure 2. (a) The schematic and (b) the timing diagram of the proposed μLED pixel circuit.

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Table 1. Electrical and geometrical parameters used for the simulation of the proposed µLED pixel circuit.

Electrical Parameters		Geometrical Parameters	
VDD	10 V	T1, T2, T4, T5, T9-T13, T15 (*W*/*L*)	4 µm/4 µm
VSS1/VSS2	-2 V/-11 V		
V_{GH}/V_{GL}	12 V/-12 V		
V_{REF}	3 V	T3, T6, T7 (*W*/*L*)	32 µm/4 µm
$DATA_{PWM}$	0 V ~ 10 V		
$DATA_{CCG}$	7 V	T8, T14, T_{CCG} (*W*/*L*)	40 µm/4 µm
SWEEP	0 ~ 9 V	C1, C2	400 fF

* *W*: width of transistor, *L*: length of transistor

In this paper, we propose a new pixel circuit that can significantly reduce the falling time of µLED current while being insensitive to V_{TH} changes using only NMOS oxide TFTs. This has a clear advantage of being able to express lower gray levels.

2. Circuit Operation

Figure 2(a) shows a pixel circuit composed of only NMOS amorphous indium gallium zinc oxide (a-IGZO) TFT. The circuit is can be divided into a PWM part and a CCG part, composed with 16 transistors and 2 capacitors. To achieve larger DC gain and output swing values, the PWM part consists of 9 transistors and 1 capacitor. Among them, 6 transistors form an NMOS inverter and C1, the storage capacitor, is used to store PWM data. The CCG part is composed of 7T1C and has a source follower structure to compensate for the V_{TH} variation of T_{CCG}. Figure 2(b) shows the timing diagram. The simulation is performed for a display panel with a 120 Hz frame rate and 480 × 270 resolution. The operation of the proposed circuit is divided into four stages: (1) PWM Data input and V_M compensation, (2) CCG Initialization, (3) CCG Data input and V_{TH} compensation, and (4) emission.

(1) PWM Data input and V_M compensation stage

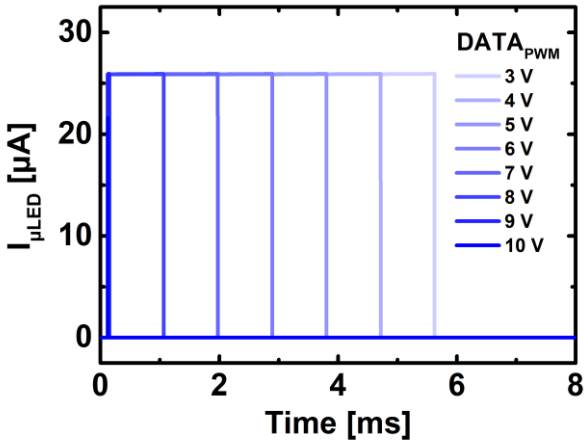
In this stage, SCAN1[n] goes high, and $DATA_{PWM}$ is applied to the left node of C1. At the same time, the right node is connected to both the input and output nodes of the inverter, which extracts the transition voltage of the inverter (V_M). Therefore, a specific voltage is applied across C1 to set its initial voltage difference, while simultaneously storing the voltage difference ($DATA_{PWM} – V_M$) in the capacitor.

(2) CCG Initialization stage

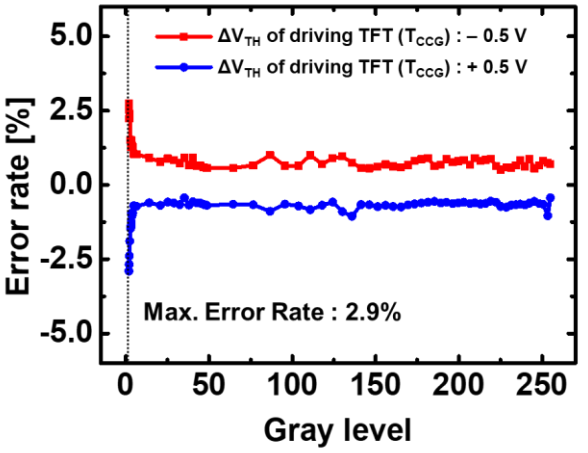
In the CCG initialization stage, SCAN1[n] is lowered to V_{GL}, while SCAN1[n+1] and SCAN2[n] are increased to V_{GH}, turning on T10, T11, and T15. As a result, the $DATA_{CCG}$ and GND voltages are applied to the left and right nodes of C2, respectively, initializing the voltage stored in C2.

(3) CCG Data input and V_{TH} compensation stage

After CCG initialization is completed, SCAN2[n] maintains a high voltage while SCAN1[n+1] transitions to V_{GL}, turning off T15. As a result, the right node of C2 enters a floating state, and current flows through T_{CCG} to charge it. Once the voltage reaches $V_{REF} – V_{TH}$, T_{CCG} turns off, leaving the capacitor with a voltage of $DATA_{CCG} – (V_{REF} – V_{TH})$.



(a)



(b)

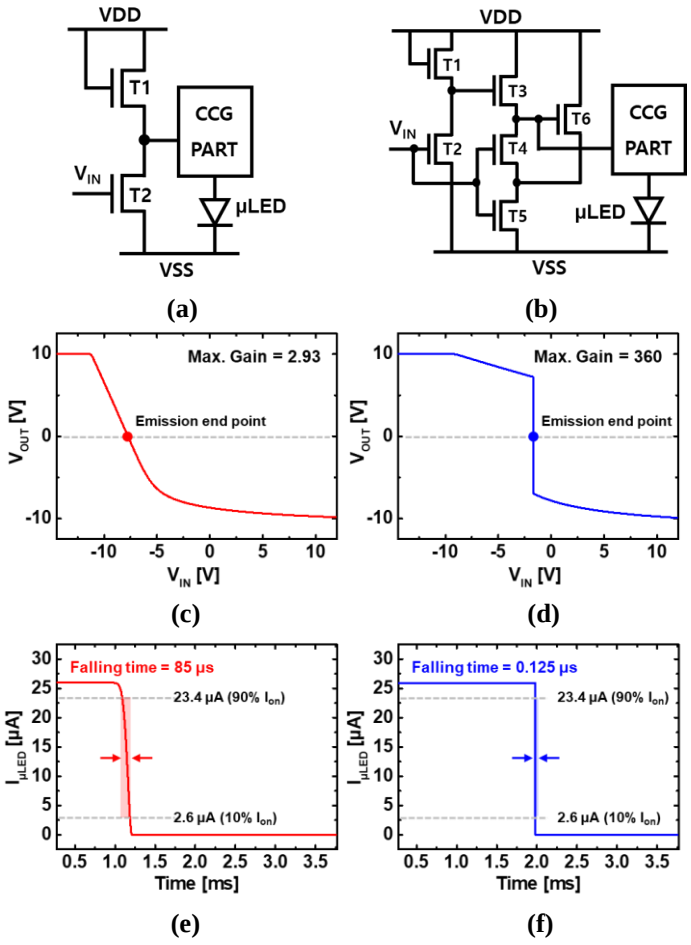
Figure 3. (a) Simulated transient waveform of µLED current and (b) the average current error rates corresponding to gray levels when the V_{TH} of T_{CCG} shifts by ±0.5 V.

(4) Emission stage

In the emission stage, SCAN2[n] decreases and EM[n] increases at the same time, turning off T10 and T11 and turning on T12 and T14. At the same time, the $DATA_{CCG}$ voltage is applied to the T_{CCG} gate and the $V_{REF} – V_{TH}$ voltage is applied to the source node of T_{CCG}, so the constant current flows as indicated in equation (1) below, causing the µLED to emit light.

$$\begin{aligned} I_{\mu LED} &= \frac{1}{2}\mu_n c_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \\ &= \frac{1}{2}\mu_n c_{ox}\frac{W}{L}\{(DATA_{CCG} - V_{REF} + V_{TH}) - V_{TH}\}^2 \\ &= \frac{1}{2}\mu_n c_{ox}\frac{W}{L}(DATA_{CCG} - V_{REF})^2 \end{aligned} \quad (1)$$

According to equation (1), the current flowing through the µLED is independent of the threshold voltage of T_{CCG}, where μ_n is the carrier mobility, c_{ox} is the capacitance of the gate oxide, and W/L is width/length of the device. Simultaneously, T2 turns on and a gradually decreasing SWEEP signal is applied to the left node of C1, with the SWEEP – ($DATA_{PWM} – V_M$) as the voltage input to



*I_{ON}: On-state current of the $I_{\mu LED}$

Figure 4. Simplified μLED pixel circuit structures featuring (a) a conventional NMOS inverter and (b) a modified NMOS inverter, with their corresponding voltage-transfer curves shown in (c) and (d), and output current characteristics in (e) and (f), respectively.

$$SWEEP - (DATA_{PWM} - V_M) < V_M \qquad (2)$$

$$SWEEP < DATA_{PWM}$$

the inverter. When the input voltage drops below V_M, as shown in equation (2), output voltage of the inverter switches to a high level, turning on T13 and stopping the light emission. Therefore, μLED emission time depends on the SWEEP signal, and the proposed pixel circuit effectively compensates for V_M variation.

3. Simulation Result and Discussion

To verify the operation of the proposed circuit, HSPICE simulations were conducted based on an a-IGZO TFT model fitted using the level 62 RPI model. The V_{TH}, mobility, and subthreshold swing (SS) of the fabricated a-IGZO TFTs were extracted from measurement data, with values of -0.29 V, 17.7 $cm^2/V{\cdot}s$, and 81.6 mV/dec, respectively.

Figure 3(a) shows the simulation result of the μLED current with various $DATA_{PWM}$. The μLED current value is fixed to 26.6 μA, and the gray level expression is successfully performed through PWM. In this study, the maximum emission time is 8.24 ms when the $DATA_{PWM}$ is 0 V, and the minimum emission time is the point when it becomes equal to the falling time. Here, the falling time is approximately 0.125 μs, remarkably shorter than the tens of microseconds seen in conventional circuits [18]-[19]. Figure 3(b) shows the average current error for each gray level when the T_{CCG} corresponding to the driving transistor of the proposed circuit is shifted by ±0.5 V. When $DATA_{PWM}$ = 10 V, the emission time is 0.125 μs, which is the same as the falling time. In this case, only an error rate of 5% was exhibited at 2-gray levels, which shows that the low-gray level expression is well achieved along with the driving TFT compensation.

Table 2. Geometrical parameters used in the inverter circuit simulation.

Conventional NMOS Inverter		Modified NMOS Inverter	
T1	4 μm/4 μm	T1	32 μm/4 μm
T2	40 μm/4 μm	T2, T3	4 μm/4 μm
		T4, T5	32 μm/4 μm
		T6	40 μm/4 μm

* *W*: width of transistor, *L*: length of transistor
** VDD: 10 V, VSS: –11 V

To assess the impact of inverters composed solely of n-type TFTs on the μLED current falling time, the modified inverter is compared with a conventional 2T NMOS inverter, demonstrating improved performance in reducing the falling time. Figure 4(a) shows a basic 2T NMOS inverter structure using a diode-connected T1 as a pull-up transistor. The width and length of the TFTs are T1 = (4 μm/4 μm) and T2 = (40 μm/4 μm). Figure 4(b) shows a modified 6T inverter used in the proposed circuit. Table 2 provides the transistor sizes for both inverters. Figure 4(c) and (d) show the voltage-transfer characteristics (VTC) of the basic NMOS inverter and the proposed inverter. Since the V_{TH} of the transistor used is -0.29 V, it is in the depletion operation state, and therefore the high-inverter output voltage (V_{OH}) of both inverters goes up to VDD. However, in the case of the low-inverter output voltage (V_{OL}), the pull-up transistor is not completely turned off like in the CMOS inverter, so it does not go down to VSS. Figure 4(e) and (f) show the μLED current when each inverter is applied to the PWM part. When using the basic 2T inverter, the falling time is about 85 μs. In contrast, the proposed modified inverter achieves a significantly reduced falling time of 0.125 μs, owing to the steep slope at the transition point.

Meanwhile, the high gain of the proposed inverter is attributed to the T4 transistor in Figure 4(b), which can be explained through the operation of the inverter: 1) when a high-voltage sweep signal is applied, T1, T2, T4, and T5 turn on. This causes a low VSS voltage to be applied to the gates of T3 and T6, turning them off and resulting in a low output voltage (V_{OL}). 2) As the sweep signal gradually decreases, the gate-source voltage of T4 (V_{GS4}) also decreases. Once V_{GS4} drops below the threshold voltage of T4 (V_{TH4}), T4 turns off, and the gate voltage of T6 enters a floating state. Simultaneously, the gate voltage of T6 rises due to the gate-source overlap capacitance component of T3, turning on T6. In this process, the inverter output voltage transitions become sharp when V_{GS4} drops below V_{TH4}, resulting in a high gain. 3) Finally, as the sweep signal continues to decrease, T2 and T5 turn off and T3 turns on. This makes the output voltage at a high level (V_{OH}). The notable point is that each inverter transistor may have different V_{TH} values, which can cause additional V_M variation. To ensure stable circuit operation, additional compensation methods should be considered.

4. Conclusion

In this paper, we proposed a circuit that significantly reduces the falling time using only NMOS-based oxide TFTs. This improvement was achieved by introducing a modified NMOS inverter structure into the μLED pixel circuit, which significantly increased the slope of the signal at the transition point of the T_{CCG} input. As a result, the circuit demonstrated enhanced performance in representing low gray levels. Notably, the proposed circuit is capable of accurately representing up to 2 gray levels with an error rate within 5%, which represents a significant improvement over the previous μLED pixel circuits. Furthermore, the performance could be further improved by implementing additional compensation methods for the internal TFTs of the inverter.

5. Acknowledgements

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