A Novel 5T2C LTPO Pixel Circuit for MicroLED Display with Simultaneous Compensation and Programming

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Abstract

We propose a new 5T2C pixel circuit for micro light-emitting diode (μLED) mobile displays. The 5T2C circuit is based on low-temperature polycrystalline silicon and metal-oxide (LTPO) thin-film transistor (TFT) technology. The proposed circuit is conducted by two methods; one is simultaneous threshold voltage compensation and data programming using double-gate oxide TFT and the other is digital driving using a stepwise signal. The simulation results show achieving full gray level and a current error rate below 2% under ±0.5 V threshold voltage variations of driving transistor and emission transistor .

Author Keywords

μLED; LTPO; pixel circuit; 5T2C; double-gate oxide TFT; simultaneous compensation and programming; a-IGZO

1. Introduction

μLED displays have emerged as a next generation display technology due to its longer lifetime, fast response time, and higher energy efficiency compared to OLED displays [1]. However, μLED displays must address a technical challenge. It has been reported that the centroid wavelength during emission can be varied depending on the amplitude of the driving current. Thus, to prevent wavelength shift, gray levels should be represented using pulse width modulation (PWM) driving instead of pulse amplitude modulation (PAM) driving, which is commonly used in OLED displays. PWM driving methods for μLED pixel circuits using sweep signals have been proposed [2], [3]. Therefore, the conventional μLED pixel circuits consist of PWM unit and constant current generation (CCG) unit. The driving transistor acting as the CCG and the emission transistor to control PWM through the sweep signal require to independently compensate for threshold voltage (V_{TH}) variation. Consequently, additional circuit elements in each pixel should be required for the V_{TH} compensation compared to conventional AMOLED pixel circuits.

Our research group has proposed the PWM driving method using a stepwise signal to reduce the circuit elements for compensation [4]. The emission transistor can be controlled by a large instantaneous gate voltage difference, reducing the effect of V_{TH} variation on the emission transistor. As a result, the circuit can operate with a low current error rate even without V_{TH} compensation for emission transistor. In this paper we adopt the proposed stepwise signal to configure the PWM unit with quaternary digital driving, aiming to design a compact pixel circuit suitable for mobile displays.

In addition, we propose a new concept to compensate for the CCG unit. A double-gate oxide TFT is utilized, and a mirror structure with an adjacent TFT is also adopted in the CCG unit, enabling simultaneous compensation and programming

Meanwhile, LTPO was employed to optimize the performance of each transistor. LTPS provides high mobility but suffers from low current stability at high temperatures due to thermionic field emission via grain boundary [5].

Oxide TFT such as amorphous-InGaZnO (a-IGZO) has better current stability at high temperatures due to its wider bandgap energy, but V_{TH} can be negative, leading to potential depletion mode operation [6].

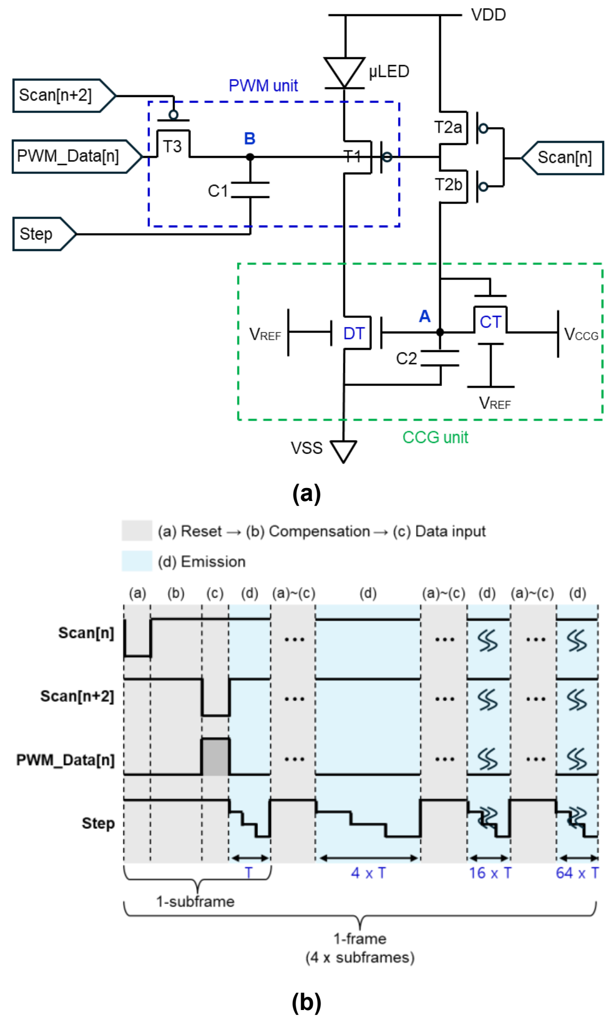

Figure 1. (a) Circuit schematic and (b) Timing diagram

2. Proposed Pixel Circuit

Figure 1 shows the circuit schematic and timing diagram. The proposed circuit consists of 5 transistors (T2a, T2b are stacked transistors) and 2 capacitors. And controlled by 3-AC signals

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(Scan, PWM_Data, Step) and 4-DC signals (VDD, VSS, V_{REF}, V_{CCG}).

In proposed circuit, switching transistors (T1, T2, T3) are implemented with PMOS LTPS TFTs to achieve low resistance and stable high-voltage output. Driving transistor (DT) and compensation transistor (CT) are designed with NMOS double-gate oxide TFTs for improved current stability at high temperatures, and to achieve simultaneous threshold voltage compensation and data programming.

The circuit can be divided into two units, the CCG unit, which drives a constant current based on the programmed voltage at node A through driving transistor DT and the PWM unit, where the voltage at node B changes according to the step signal to control the on and off timing of emission transistor T1.

As a quaternary digital driving method, one frame consists of four subframes, and each subframe comprises (a) Reset, (b) V_{TH} compensation, (c) Data input, and (d) Emission phases. In all subframes, the phase times for (a) ~ (c) are identical for 5 µs, 25 µs, and 5 µs, respectively. However, in the (d) Emission phase, the timing increases by a factor of 4 for each subframe, resulting in timings of 1T (15µs), 4T (60µs), 16T (240µs), and 64T (960µs). Below is a description of the operations for each phase within a subframe.

(a) Reset phase
When Scan[n] becomes low, T2 turns on. Node A and node B are reset to VDD, and T1 turns off, preventing µLED emission.

(b) Compensation phase
When Scan[n] becomes high, T2 turns off, and node A is programmed with the voltage $V_{TH,CT}$ + V_{CCG} through the diode connection of CT. $V_{TH,CT}$ refers to the V_{TH} of CT.

(c) Data input phase
When Scan[n+2] becomes low, T3 turns on. And then, V_{PWM_Data} is stored in node B, which is bigger than $V_{TH,T1}$ keeping T1 off.

(d) Emission phase
When Scan[n+2] becomes high, T3 turns off. Simultaneously, Step signal decreases in three stages, causing the gate voltage of T1, coupled via C1, to drop by an equal amount at each stage. The pulse width of emission current is controlled by varying V_{PWM_Data} across subframes, enabling the representation of 8-bit gray levels.

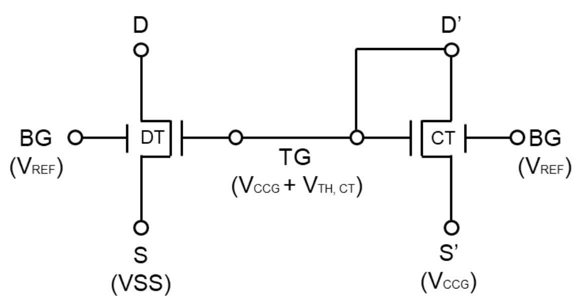


Figure 2. Concept of simultaneous threshold voltage compensation and data programming

Figure 2 shows the concept of simultaneously performing threshold voltage compensation and CCG data programming within the CCG unit.

$$V_{TH,DT} = V_{TH}(0) + \beta(V_{BG} - V_S) \quad (1)$$

$$V_{TH,CT} = V_{TH}(0) + \beta(V_{BG} - V_{S'}) \quad (2)$$

$$\Delta V_{TH} = V_{TH,CT} - V_{TH,DT} = \beta(VSS - V_{CCG}) \quad (3)$$

In case of a double-gate a-IGZO TFT, the threshold voltage of DT, $V_{TH,DT}$ is expressed as equation (1), the threshold voltage of CT, $V_{TH,CT}$ is expressed as equation (2) and the difference ΔV_{TH} is expressed as equation (3) [6].

Where β is $-\frac{C_{BI}C_{IGZO}}{C_{TI}(C_{BI}+C_{IGZO})}$, $V_{TH}(0)$is considered as the TFT's threshold voltage for BG voltage V_{BG} = 0V [6].

$$I_{DS} = \frac{1}{2}k(V_{TG-S} - V_{TH,DT})^2 = \frac{1}{2}k(V_{CCG} - VSS + \Delta V_{TH})^2$$
$$= \frac{1}{2}k[(1-\beta)(V_{CCG} - VSS)]^2 \quad (4)$$

Equation (4), derived from Equation (3) and the TFT current equation in the saturation region, represents the current of DT. β is determined by the thickness of a-IGZO and the gate insulator, and it is expected to exhibit high uniformity over short range. Therefore, the circuit can drive the constant current even with variations in the V_{TH} of the driving TR.

Since V_{CCG} is set to a voltage higher than V_{REF}, $V_{TH,CT}$ has a negative V_{BG}-V_S, allowing diode connection of CT to operate in enhancement mode with a positive $V_{TH,CT}$ even if $V_{TH}(0)$ is under negative bias.

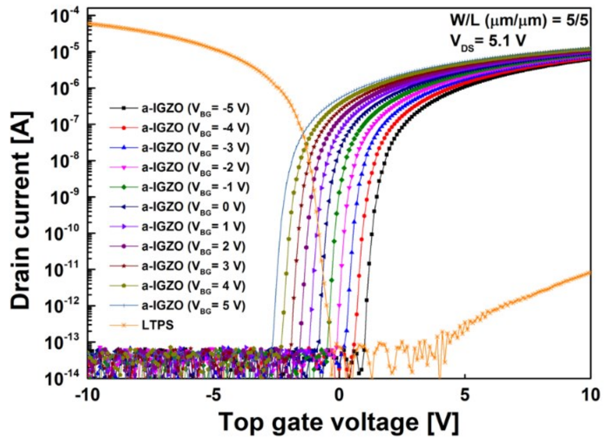
3. Results and Discussion

The proposed µLED pixel circuit operation was investigated using the circuit simulation (SmartSpice, Silvaco). The circuit parameters are listed below in Table 1.

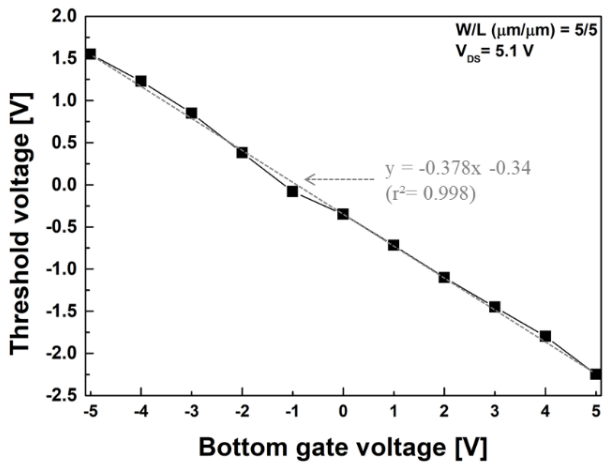
Table 1. Circuit parameters.

Parameter values			
W/L of DT, CT	6 µm/6 µm	V_{REF}	-2 V
W/L of T1	15 µm/3 µm	V_{CCG}	2 V
W/L of T2, T3	3 µm/3 µm	Scan	-5 ~ 23 V
C1/C2	0.2pF/0.4pF	V_{PWM_Data}	3, 8, 15, 23 V
VSS/VDD	0 V/7 V	Step	-8, -3, 2, 7 V

DT and CT are designed with equal width and length to ensure they have the same threshold voltage. T1 was designed with a width of 15 µm and a minimum length (3 µm) to achieve low resistance. T2 and T3, as they are not part of the emission current path, were both designed with minimum width and length (3 µm/3 µm).



(a)



(b)

Figure 3. Measured (a) Transfer characteristics of double gate a-IGZO TFT and LTPS TFT, and (b) V_{TH} variation with the bottom gate voltage V_{BG} of double gate a-IGZO TFT

Figure 3(a) shows the transfer characteristics of double-gate a-IGZO TFT and LTPS TFT, measured for TFT modeling for circuit simulation. In the case of double-gate a-IGZO, C_{BI} = 1.844×10^{-2} F/m^2 , C_{TI} = 2.466×10^{-2} F/m^2, C_{IGZO} = 1.771×10^{-2} F/m^2, resulting in a $\beta_{calculated}$ = -0.366.

Figure 3(b) shows the graph of V_{TH} by varying with V_{BG} for the double-gate a-IGZO. The slope of the linear function, indicated by the dashed line, is -0.378. According to Equation (1), the slope corresponds to $\beta_{measured}$. Therefore $\beta_{measured}$ = -0.378. $\beta_{calculated}$ - $\beta_{measured}$ is 0.011, demonstrating strong agreement between the theoretically predicted V_{TH} shift and the experimentally measured data.

In the proposed circuit, V_{BG} of CT, achieved through diode connection for simultaneous threshold voltage compensation and data programming, is V_{REF} - V_{CCG}, which is -4 V. Based on the $\beta_{calculated}$, $V_{TH, CT}$ = V_{TH} (0) +1.464 V. This suggests that even if the initial V_{TH} of the double-gate a-IGZO TFT is negative, the proposed structure can enable CT to operate in enhancement mode.

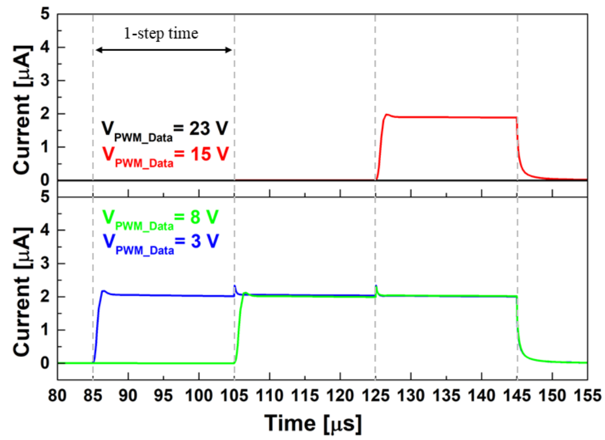


Figure 4. Simulated μLED emission current within a single subframe by different V_{PWM_Data}

Figure 4 shows the μLED emission current over time within a single subframe, determined by various V_{PWM_Data}. When the V_{PWM_Data} is set to 3 V, 8 V, 15 V, and 23 V, the subframe emission time corresponds to 3 times, 2 times, 1 time, and 0 times the 1-step time, respectively.

During the emission phase, a step signal decreases by -5V at each 1-step time. Due to the capacitance coupling effect of C1, the voltage at node B, which is the gate node of transistor T1, is dynamically changed. If the voltage at node B exceeds the threshold voltage of T1, the transistor switches on, enabling the emission of the μLED. Conversely, when the voltage is below the threshold, T1 remains off, suppressing μLED emission.

The four subframes have emission times of 1T (15μs), 4T (60μs), 16T (240μs), and 64T (960μs). By combining these subframes with V_{PWM_Data}, the system can represent 256 gray levels within a single frame.

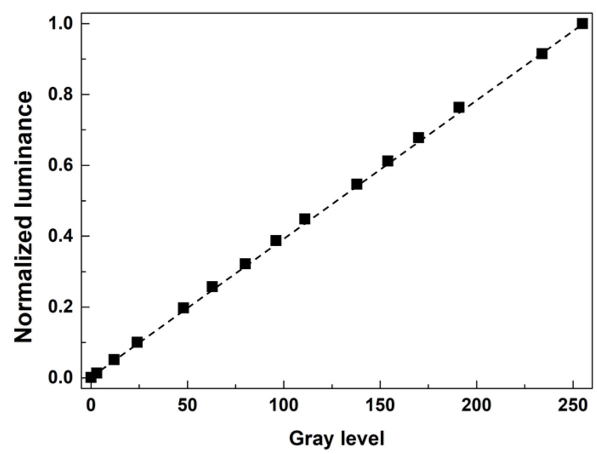


Figure 5. Simulated luminance over gray level from 0~255 gray level.

Figure 5 shows the integrated μLED current over the total emission time for each gray level. By defining the luminance at the maximum gray level as 1, the normalized luminance exhibits a linear characteristic, as shown in the figure. This confirms that the proposed circuit can achieve 8-bit digital driving.

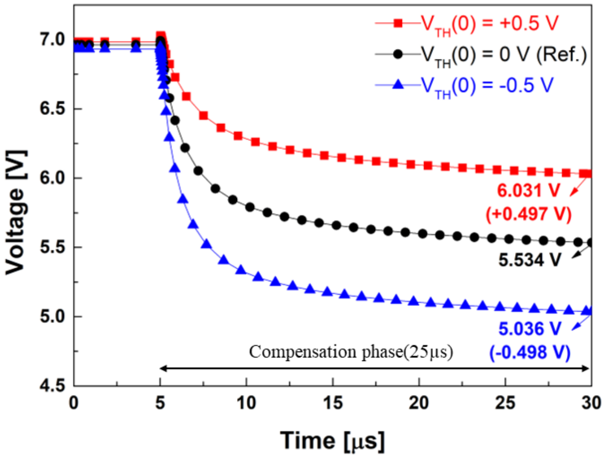


Figure 6. Simulated node A voltage during compensation phase under $\mathbf{V_{TH}(0)}$ of DT and CT set to -0.5 V, 0 V, +0.5 V.

Figure 6 shows the voltage of node A during the compensation phase as the threshold voltage of DT and CT set to -0.5 V, 0 V, 0.5 V. Since $\beta(V_{BG} - V_{S'}) < 0V$, $V_{TH,\,CT} > 0V$, enabling CT to operate in enhancement mode, allowing simultaneous compensation and programming through the diode connection of CT.

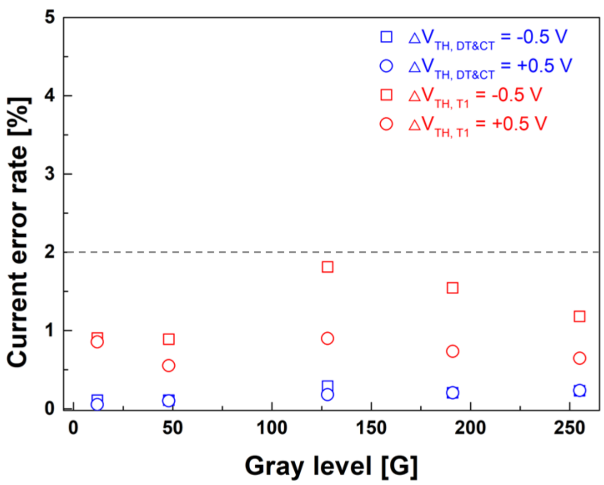


Figure 7. Simulated μLED emission current error rate under V_{TH} variation of ±0.5 V for DT&CT, T1

Figure 7 shows the current error rate, which remains below 2% across all cases. The low error rate for variations in $V_{TH,\,DT\&CT}$ can be attributed to the compensation mechanism, as discussed in the previous paragraph. In the case of variation in $V_{TH,\,T1}$, the low error rate is due to the sufficiently large voltage change in the step signal, which mitigates the impact of $V_{TH,\,T1}$ on the emission time.

4. Conclusion

We designed a μLED pixel circuit using only 5T2C, incorporating simultaneous compensation and programming for threshold voltage compensation and a stepwise control signal for PWM driving. The circuit was validated through spice simulations.

First, by controlling the PWM data, we verified the feasibility of 8-bit digital driving by analyzing the μLED emission current waveform over time and the luminance at different gray levels.

Second, we verified that the circuit operates effectively even when a-IGZO TFTs exhibit negative V_{TH}. This was demonstrated by the voltage stored at node A when $V_{TH}(0)$ of DT and CT were set to -0.5 V, 0 V, and 0.5 V.

Consequently, the circuit maintained a current error rate below 2% under V_{TH} variations of ±0.5 V for DT&CT and T1.

In conclusion, the proposed 5T2C μLED pixel circuit demonstrates stable 8-bit digital driving even under the threshold voltage variations of both the CCG unit transistors and the PWM unit transistors.

5. References

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