Achieving High-Performance Ln-IZO TFT with Top-Gate Self-Aligned Structure on Large Substrates

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Abstract

This paper discusses the strategy for achieving high performance Ln-IZO TFT utilizing a top-gate self-aligned (TGSA) structure on a G8.6 glass substrate. We examined the PECVD process of the GI layer, focusing on plasma power and post-treatment, to reduce the interface trap states between the GI and active layer. The premium Ln-IZO TFT exhibited a mobility of 47.3 cm²/Vs, a subthreshold swing (SS) of 0.30, a threshold voltage (Vth) of 0.35 V, and an on/off current ratio (Ion/Ioff) of 2.3×10⁹. The BTS stability of Ln-IZO TFT is also within 1.0 V (PBTS = 0.76 V, NBTIS = 0.48 V), indicating significant market potential for next-generation display devices.

Introduction

Amorphous oxide semiconductors (AOS) have garnered considerable attention owing to their high mobility and transmittance in the visible spectrum, as well as its potential for large-area fabrication. Nonetheless, the bias stress stability issue (BTS) constantly inhibits the very best implementation of AOS in the display industry, particularly concerning positive bias temperature stability (PBTS) and negative bias temperature illumination stress (NBTIS) stability. Balancing the trade-off between high mobility and stability in materials design is challenging.

Recent reports indicate that Lanthanide doping can effectively suppress photoelectrons by rapid recombination, hence enhancing the stability of light-sensitive oxide thin-film transistors (TFTs). However, the stability of PBTS continues to impede its application. Inversely, the fabrication process can also be a task. Threp principal types of a-IGZO TFT structures employed for display backplanes are back channel etch (BCE), top-gate (TG), and top-gate self-aligned (TGSA) structures. The TGSA oxide TFT structure effectively prevents parasitic capacitance, benefiting high-speed, low-power devices, especially OLED displays. The fabrication of the TGSA structure, especially the GI layer and the conductive process of the active layer, may result in increased interface defects, resulting in negatively impacting the stability of the BTS.

This study applies lanthanide-doped IZO as the channel layer in the TGSA structure TFT due to its strong bonding energy with oxygen. We examined the parameters of the CVD process to decrease the interface trap state. In the end, High-performance AOS TFTs have been successfully developed on large substrates.

Experimental

Figure 1 illustrates the cross-sectional diagram of the TGSA Ln-IZO TFT structure employed in this research. The devices were manufactured on a G8.6 (2290 mm x 2620 mm) glass substrate. Initially, PECVD was utilized to deposit a 30 nm SiN_x layer and a 220 nm SiO_2 buffer layer. A 20 nm thick Ln-IZO film was deposited via DC magnetron sputtering at ambient temperature. The GI layer comprised 150 nm of SiO_2 produced via PECVD, followed by dry etching to provide via holes for connecting the Gate with Ln-IZO and SD. The MoTi/Cu gates were deposited via DC magnetron sputtering and subsequently patterned using photolithography and copper etchant. A passivation layer of SiO_2 and SiN_x was finally applied to safeguard the TFT channel and metal layer. The electrical performance of the TFT was assessed using a semiconductor characteristics analyzer. The initial properties of TFTs, positioned at four distinct locations on a glass plate, were measured at room temperature in darkness with a drain voltage of 15V. A positive bias temperature stress (PBTS) test was performed at 60°C in darkness with a gate bias of 30V for 3600 seconds. The Negative Bias Temperature Illumination Stress (NBTIS) test was conducted at 60°C with a backlight illumination of 5000 nits and a gate bias of -30V for a duration of 3600 seconds. During the PBTS/NBTIS test, I-V transfer curves were obtained with VGS varying from -15 V to 25 V, while VDS was maintained at 15 V. This paper examines the various GI CVD parameters obtained from three groups of TFTs (Table 1). Device A/B/C derived from group 1/2/3.

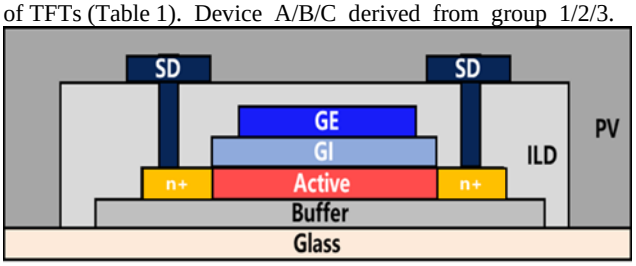

Fig. 1. Cross-sectional diagram of the SATG structure Ln-IZO TFT.

Results and Discussion

Figure 2(a) shows the I_D-V_G characteristics of Ln-IZO device structure with different GI CVD parameter on G8.6 panel glass. The group-1 exhibits the mean V_{th} of -3.9 V, u_{FE} of 39.1 cm^2/Vs, SS of 0.39 V/decade. The V_{th} distribution range of G8.6 glass is 5.2 V. With shorter dry etch plasma time, the uniformity of group-3 became better, presented u_{FE} of 42.1 cm^2/Vs, SS of 0.35 V/decade. The V_{th} distribution range is 0.2 V. When lower the GI plasma, u_{FE} of 47.3 cm^2/Vs, SS of 0.30 V/decade. The V_{th} distribution range is 0.1 V. Such improvement of TFT stability might mainly result from better attachment of GI onto Ln-IZO and less interface and bulk defects in low-power deposited GI layer.

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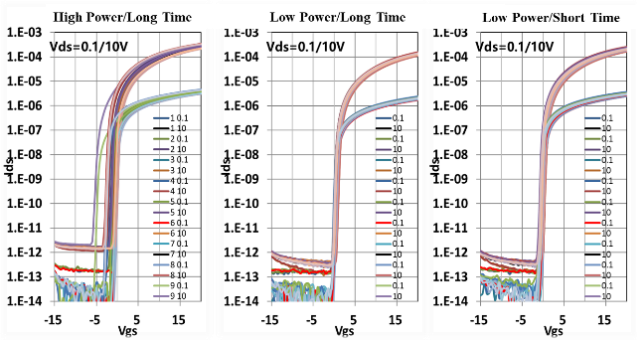


Figure 2. The ID-VG characteristics of Ln-IZO device structure with different GI CVD parameter on G8.6 panel

Table 1. Extracted electrical parameter of Ln-IZO TFTs

		Group 1	Group 2	Group 3
Condition	**Power**	**High**	**High**	**low**
	Time	Long	short	short
Characteristic	**u_{FE}**	42.1	39.3	47.3
	SS	0.39	0.35	0.30
	Range	3.9	0.5	0.3

The PBTS stability results of different Ln-IZO TFTs are depicted in figure 2. The Device A PBTS stability average is 4.2 V, the Device B is 0.76 V, the Device C is 0.46 V. The positive drift of the Vth is due to the injection of electrons at the interface; thus, the charge trap model is used to evaluate the PBTS stability.

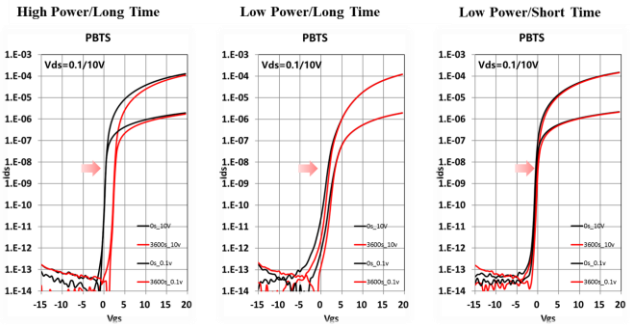


Figure 2. The PBTS stability results of different conditi ons.

The stretched-exponential equation for the ΔV_{th} is defined as:

$$\Delta V_{th} = \Delta V_{th0}\left[1 - exp\left\{-\frac{t}{\tau}\right\}^{\beta}\right]$$

where ΔV_{th0} is the ΔV_{th} at infinite time, t is stress time, τ represents the characteristic trapping time of carriers, and β is the stretched-exponential exponent correlated with the energy barrier. In general, decreased shift of V_{th0} implies the injection barrier will be higher (β will be smaller) and the trapping time τ required to reach ΔVth0 will be longer. Our results show an increase in τ (from 0.6 to 5.3 $\times 10^3$ s) and a decrease in β (from 0.6 to 0.49) after optimizing CVD parameter, which points out that the less interface traps in Device C.

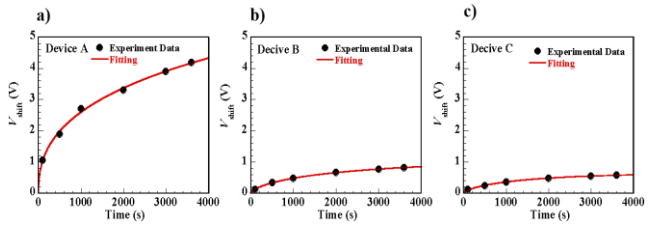


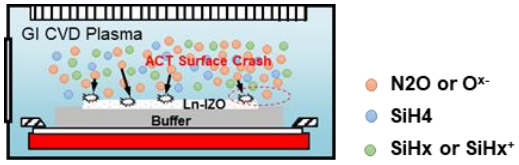
Figure 3. The stretched-exponential fitting of ΔV_{th} of a) Device A; b) Device B; c) Device C.

Table 2. Results of expanded exponential Model Fitting of ΔV_{th}

Device ID	ΔV_{th0} (V)	τ ($\times 10^4$ s)	β
A	15.1	0.6	0.60
B	7.8	4.6	0.54
C	1.3	5.3	0.49

the widely accepted explanation for the formation PBTS is the excess oxygen (Oi) in the band gap upon electrical field, followed by the electron accumulation at the interface under an electric field. When the plasma power decrease, the damage to channel also decreases. In addition, N_2O plasma treatment also decrease oxygen vacancy by supplying oxygen. Finally, optimized GI CVD process can effectively decrease interface defect state thus decreasing the ΔVth in PBTS test.

(a)



(b)

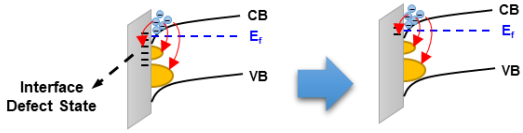


Figure 4. The schematic diagram of improvement of BTS stability by interface defect control.

Conclusion

In this paper, various dry etch methods have been applied to create high conductive area of Ln-IZO active layer in top gate structure. By adjusting GI CVD parameter (plasma power and time), a short channel length (W/L=6/4 um) TFT has successfully obtained in G8.6 line, with mobility of 47.3 cm^2/ Vs, SS of 0.30, Vth of 0.35 V, I_{on}/I_{off} of 2.3×10^9. In addition, the BTS stability of Ln-IZO TFT within 1.0 V (PBTS=0.76 V, NBTIS=0.48 V), which can provide extensive market potential in next generation display device.

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