Poster P-128 has been designated as a Distinguished Poster at Display Week 2025. The full-length version of this paper appears in a Special Section of the *Journal of the Society for Information Display (JSID)* devoted to Display Week 2025 Distinguished Papers. This Special Section will be freely accessible until December 31, 2025 via:

https://sid.onlinelibrary.wiley.com/doi/full/10.1002/jsid.2053

Authors that wish to refer to this work are advised to cite the full-length version by referring to its DOI:

https://doi.org/10.1002/jsid.2053

A 1.33 μV/e⁻ Voltage Mode Active Pixel Sensor with Threshold Voltage Compensation for Dynamic X-Ray Imaging

Jiangbo Hu, Yuhan Zhang*, Congwei Liao*, Xiaoliang Zhou**, Hejing Sun**, Zhiwei Tan**, and Shengdong Zhang**

*School of Electronic and Computer Engineering, Peking University, Shenzhen, 518055, China

**TCL China Star Optoelectronics Technology Co. Lth, Shenzhen, 518132, China

Abstract

This paper proposes a high-gain voltage-mode active pixel sensor (V-APS) for high-frame-rate dynamic X-ray imaging. Due to a source-follower structure, the proposed active pixel circuit exhibits superior linearity compared to current-mode APS. And, a shared programmable gain amplifier (PGA) is employed to provide secondary-stage amplification, mitigating the gain limitation of the source-follower structure. The charge-to-voltage gain of the proposed V-APS achieves 1.33 μV/e⁻ with a nonlinearity of 0.38%. Furthermore, V_T variation and shift of amplifying transistors in pixels and PGAs can be compensated by using dual-gate thin-film transistor technology. In comparison with conventional 3-T V-APS, the proposed one features a significant decrease of output voltage error rate from 43.67% to 0.79% at a V_T shift of ±0.5 V.

Author Keywords

Voltage-mode active pixel sensor (V-APS); Source-follower structure; Shared programmable-gain; Dual-gate thin-film transistor (DG TFT); Negative threshold voltage compensation.

1. Introduction

Current-mode active pixel sensor (C-APS) is currently the mainstream scheme in large-area flat-panel X-ray imaging [1]. Since both the reference voltage on the data bus and the output current are constant, C-APS scheme can avoid the impact of RC delay and enables the high readout frame rate. However, C-APS exhibits poorer linearity compared to voltage-mode active pixel sensor (V-APS) due to the nonlinear relationship between the input signal and the output current [2].

In addition, C-APS imposes tough specs on the external readout ICs (ROICs) [1], [2]. One architecture of ROIC is based on integrators [1], which require large capacitors (typically greater than 30 pF per channel), making them cost-ineffective for large-area X-ray imaging. The other ROIC approach, based on transimpedance amplifiers [2], introduces additional noise and suffers from more severe mismatch issues compared to integrators. However, the ROIC architecture for V-APS typically only requires buffers instead of complex integrators or transimpedance amplifiers, making it more cost-effective and avoiding the mismatch of capacitors or resistors.

V-APS has been widely adopted in complementary metal oxide semiconductor (CMOS) image sensors [3]. Nevertheless, V-APS is unsuitable for imaging sensors of large-area X-ray flat-panel detectors (FPD) based on amorphous silicon technology, which is currently mainstream for FPD applications. This limitation stems from the relatively long settling time of the output voltage due to low mobility and large parasitic capacitance on the data bus. Previous studies demonstrated methods to reduce the settling time of V-APS by utilizing high-mobility TFT, such as amorphous indium tin zinc oxide (a-ITZO) and low temperature poly-silicon (LTPS) [4], [5]. However, these approaches cannot provide a high-gain and flexible programmability. Additionally, the amplification function has the instability concern, as the amplifying TFTs are prone to long-term electrical bias and/or are nonuniform among channels. As a result, the reliability of V-APS remains an unresolved issue in these approaches.

This work demonstrates a novel V-APS design utilizing dual-gate TFTs with a self-aligned structure. This design results in a significantly reduced settling time on the signal bus and enables the sensor to meet the frame rate requirements for large-area X-ray imaging. Furthermore, the bias current source consists of a single TFT with high output impedance, and the programmable gain amplifier (PGA) shared by a column of pixels performs secondary-stage amplification of the input signal for higher gain and signal-to-noise ratio. In addition, negative and positive V_T of amplifying transistors in pixels and PGAs can be compensated, as they store the value of V_T by one of the gates, and the other gate is used for amplifying. Therefore, the proposed V-APS is promising for dynamic X-ray medical imaging applications.

2. Proposed APS Circuit and Operation

Figure 1 shows the schematic of the proposed V-APS. The pixel consists of two resetting TFT (T_{R1} and T_{S1}) and one amplifying TFT (T_{A_PIXEL}). The PGA shared by pixels of a column is constituted of two resetting TFT (T_{R2} and T_{S2}) and one amplifying TFT (T_{A_PGA}). T_{R2} and the storage capacitor at node C are used to compensate for threshold voltage shift (ΔV_T). T_{BIAS} is a switching TFT in the V_T extraction phase and a bias current source with high output impedance in the readout phase. The timing diagram is illustrated in Figure 2.

In the reset phase, RST_1, RST_2, SW_1, RST_3 and RST_4 are all high, and then node A and node C are charged to VDD. The voltage on the data line is equal to V_{REF}.

In the V_T extraction phase, RST_2 and RST_3 are low to turn T_{S1} and T_{S2} off. In the meantime, node A and node C are discharged through the diode connection until the transient current approaches 0 V. Consequently, the V_T of T_{A_PIXEL} and T_{A_PGA} is always set to 0 V after V_T extraction phase, no matter how it varies before. Since V_{REF} is lower than VSS and the low level of Sense[n] is higher than 0 V, the circuit is still capable of compensating for negative V_T of T_{A_PIXEL} and T_{A_PGA}.

In the global exposure phase, the photodiode (PD) is in a reverse-biased condition, and the movement of holes and electrons forms the PD photocurrent I_{PH} flowing from the PD cathode to the PD anode

ISSN 0097-996X/25/5603-1920-$1.00 © 2025

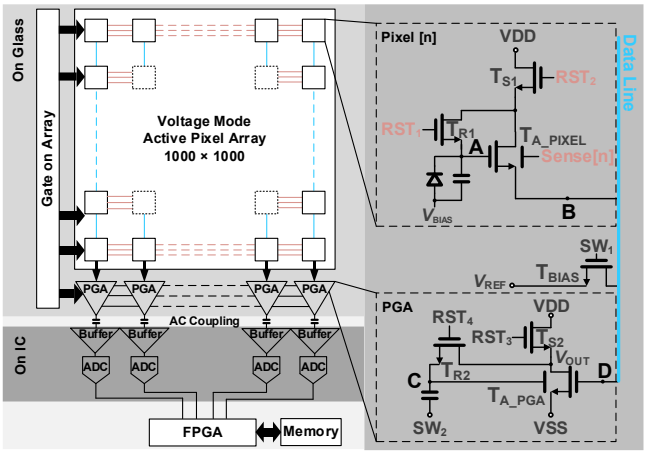

Figure 1. The proposed V-APS architecture based on DG IGZO TFT.

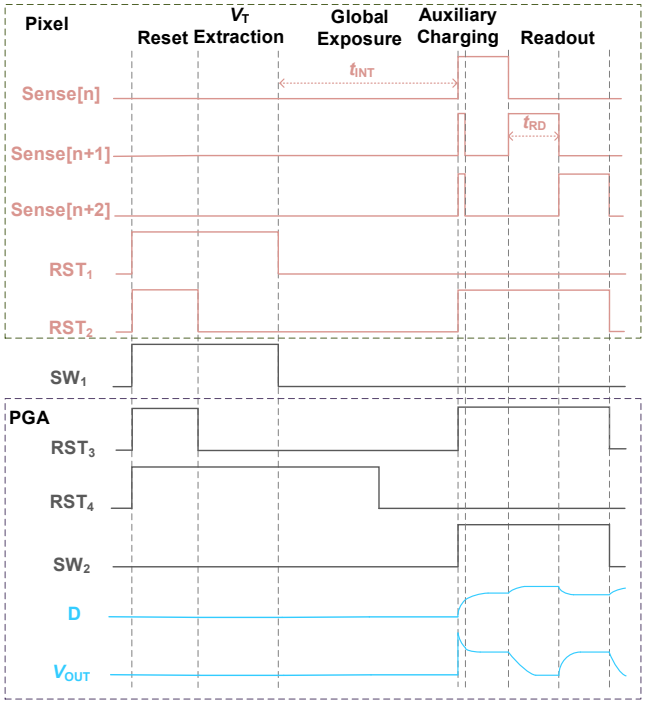

Figure 2. The timing diagram.

Therefore, the charge (ΔQ_{IN}) in the storage capacitor at node A is reduced. ΔQ_{IN} can be expressed as:

$$\Delta Q_{IN} = \int_0^{t_{INT}} I_{PH}\,dt \tag{1}$$

Here, t_{INT} is the time of global exposure. $RST_1[n]$ is low to turn T_{R1} off to prevent the leakage of data charge in C_{ST}.

In the auxiliary charging phase, Sense[2] and Sense[3] are high briefly to decrease the settling time of the first row. Then, Sense[n] is progressive for other rows in the readout phase. The voltage level of Sense[n] is elevated by ΔV_1 to increase the transconductance of T_{A_PIXEL} for higher charge-to-voltage gain (CtV gain), and SW_1 is low for making T_{BIAS} a bias current source during the readout phase. In the meantime, RST_3 is low to turn T_{S2} off. By adjusting the voltage level of SW_2, the gain of the PGA during the readout phase is programmable.

After in-pixel compensation, ΔV_{out} be expressed as:

$$\Delta V_{OUT} = G_{PGA}\Delta V_{IN} = -\frac{g_{m\_A\_PGA}}{g_{ds\_A\_PGA} + g_{ds\_S2} + g_{m\_S2}}\Delta V_{IN} \tag{2}$$

Here, G_{PGA} is the voltage gain of the PGA. g_m is the transconductance of T_{A_PGA} and T_{S2}, and g_{ds} is the output conductance of T_{A_PGA} and T_{S2}. The voltage gain of the pixel is about 1 due to the high output impedance of T_{BIAS}.

Since T_{A_PIXEL} and T_{A_PGA} have been compensated, the output voltage is independent of V_T thanks to the V_T extraction phase. This approach effectively mitigates V_T shift and nonuniform issues of T_{A_PIXEL} and T_{A_PGA}. These voltage values of the output are then transferred to the analog-to-digital converters (ADCs) through the buffers. The buffers are connected to the PGAs in AC coupling, which does not require the common-mode level of PGAs to be consistent with that of the external buffer, mitigating the limitation on ROICs.

The cost of such a readout scheme is that pixel-level hardware double sampling is not possible due to the long time of the V_T extraction phase; therefore, software double sampling must be employed. In software double sampling, the dark field image is stored in the memory and subtracted from images taken in the presence of X-ray in order to correct for any fixed pattern noise in the array and recover the signal (from the bias). If multiple dark field images are averaged, then the white noise will be considerably reduced, such that the thermal noise and reset noise of the dark field image are negligible [6]. The architecture of the software double sampling is shown in Figure 1, and the calculation between images is done in the field programmable gate array (FPGA).

3. Results and Discussions

The proposed V-APS is implemented using DG a-IGZO TFT technology, with a self-aligned structure to minimize parasitic capacitance [7], which can significantly reduce the settling time on the data line. Figure 3(a) illustrates the cross-sectional view and equivalent symbol of the DG TFT.

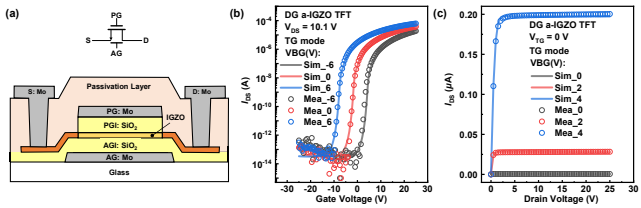

Figure 3. (a) Cross-sectional schematic of DG a-IGZO TFT and its equivalent electronic symbol. (b) Simulated and measured transfer characteristic curves of the DG a-IGZO TFT. (c) Simulated and measured output characteristic curves of the DG a-IGZO TFT.

Figure 3(c) illustrates excellent output characteristic curves of the DG a-IGZO TFT at TG mode, which indicates that the gain of pixel amplification is almost independent of the current value of T_{BIAS}. Although the DC offset of node D is related to the current, it can be eliminated by software double sampling. Consequently, the linear relationship between input and output is not affected by ΔV_T of

T_{BIAS} after software double sampling.

To achieve a pixel size of 95 × 95 μm^2 for higher resolution, the *W/L* ratio of T_{A_PIXEL} is 100 μm/6 μm, while the *W/L* ratio of T_{R1} and T_{S1} are 10 μm /6 μm. The parasitic capacitance of PD is 0.6 pF. The *W/L* ratio of T_{A_PGA} is 500 μm/6 μm, the *W/L* ratio of T_{S2} is 10 μm/20 μm, the *W/L* ratio of T_{R2} is 10 μm/6 μm, and the *W/L* ratio of T_{BIAS} is 200 μm/6 μm. The storage capacitor at node C is 3 pF. The global reset time is set to 150 μs, the V_T extraction time is 50 μs, and the global exposure time is 1 ms. Considering a typical array comprising of 1000 ×1000 pixels operating in real-time at 30 Hz, the total readout time per row is 32 μs.

3.1 CtV Gain and Linearity

The relationship between I_{PH} and V_{OUT} is illustrated in Figure 4. In the proposed circuit, the R^2 value is 0.99998, the high CtV gain is 1.33 $\mu V/e^-$, and the nonlinearity is 0.38%. According to (2), the relationship between input and output is linear in the case of the output impedance of T_{BIAS} that is large enough. On the contrary, the relationship of C-APS between the input signal and the output current is square. Therefore, the linearity has been greatly improved compared to the conventional 3-T C-APS. The CtV gain is programmable, which can be achieved by varying the value of ΔV_2. Considering a zero-point and gain calibration is required to compensate for variability and degradation anyhow [2], the problem of zero-point misalignment can be solved.

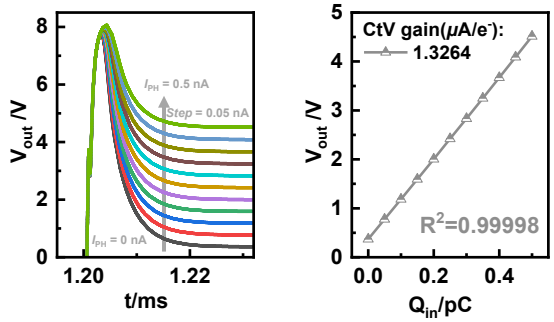

Figure 4. (a) The transient response of V_{OUT} versus different input photocurrent. (b) Relationship between the input charge and the output voltage.

3.2 Threshold Voltage Compensation

Figure 5 illustrates V_T compensation effect. The proposed active pixel circuit effectively compensates for both positive and negative V_T shifts. With I_{PH} of 0.5 nA and t_{INT} of 1 ms, the output voltage error remains within 0.79% under ΔV_T of ±0.5 V in the proposed circuit. The output voltage error rate of the voltage-mode 3-T APS without in-pixel compensation is 43.67%.

3.3 Settling Time

As illustrated in Figure 6(c), the voltage variation for the first row is greater than that of the other rows, indicating a longer settling time. In the absence of auxiliary charging, this increases the readout time of the first row by approximately 8 μs, resulting in total readout time exceeding 32 μs, as shown in Figure 6(b). As depicted in Figure 6(a), for a single pixel column, the first three rows are located farther from node D compared to other rows, leading to longer *RC* time. Consequently, assuming that the settling time of the first three rows meets the 12-bit settling accuracy requirement, other rows will inherently satisfy this criterion. As shown in Figure 6(d), the voltage variation on the data line for the first three rows remains below 0.001 V between 31.5 μs and 100 μs (between M and N), and this variation becomes negligible beyond 100 μs.

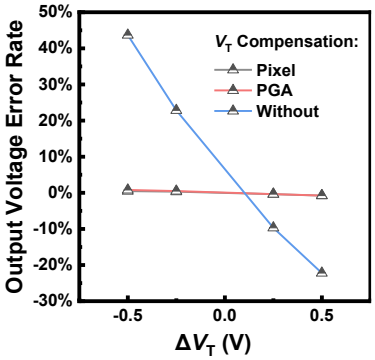

Figure 5. Compensation effect for positive and negative threshold voltage shift. The output voltage error does not exceed 0.79% under a threshold voltage shift of ±0.5 V.

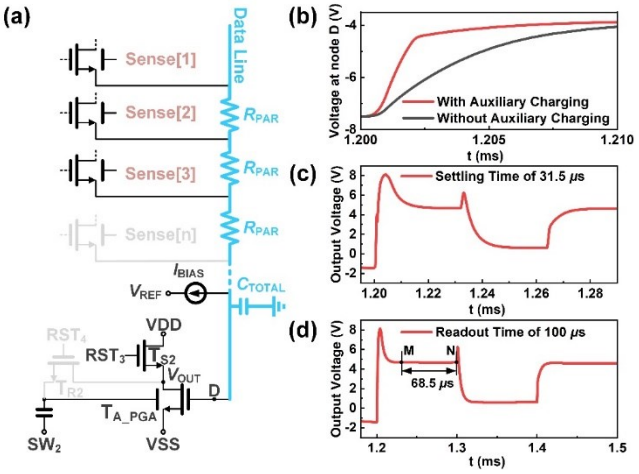

Figure 6. (a) The circuit diagram with parasitic resistance and capacitance in the auxiliary charging phase. (b) The settling time of the first row with and without auxiliary charging. (c) The settling time of the first three rows with auxiliary charging. (d) The settling accuracy of the first three rows during 300 μs.

Therefore, it can be inferred that the first three rows achieve a settling accuracy of 0.001 V by 31.5 μs. Considering the output swing of 4.125 V, the corresponding 12-bit voltage accuracy is 0.001 V. Hence, all pixels within a column can achieve the required 12-bit settling accuracy within a readout time of 32 μs.

3.4 Noise Analysis

The noise characteristics of the proposed V-APS can be categorized into pre-amplification noise and post-amplification noise. The pre-amplification noise σ_{PRE} consists of σ_{PD} (dark current of PD), σ_{TFT1} (leakage currents of T_{R1}), and σ_{RESET1} (reset noise from T_{R1} on the storage capacitor). The post-amplification noise σ_{POST} includes σ_{F1}, σ_{F2}, σ_{F3} and σ_{F4} (flicker noise) and σ_{T1}, σ_{T2}, σ_{T3} and σ_{T4} (thermal noise) from the T_{A_PIXEL}, T_{S1}, T_{A_PIXEL} and T_{S2}, σ_{RESET2} (reset noise on C_{TOTAL}), σ_{RESET3} (reset noise on the storage capacitor at node C) and σ_{AMP} (noise from the ROIC). The charge gain of the source-follower structure G_{PIXEL} is equal to C_{TOTAL}/C_{ST}. C_{ST} is the storage capacitor at node A. The input reference noise σ_{TOTAL} is expressed

as:

$$\sigma_{TOTAL} = \sqrt{\sigma_{PRE}^2 + \frac{\sigma_{F1}^2+\sigma_{F2}^2+\sigma_{T1}^2+\sigma_{T2}^2+\sigma_{RESET2}^2+\sigma_{RESET3}^2}{G_{PIXEL}} + \frac{\sigma_{F3}^2+\sigma_{F4}^2+\sigma_{T3}^2+\sigma_{T4}^2+\sigma_{AMP}^2}{G_{PIXEL}G_{PGA}}} \quad (3)$$

According to (3), the secondary-stage gain G_{PGA} significantly mitigates the impact of noise from PGA and σ_{AMP}, indicating lower σ_{TOTAL} and higher signal-to-noise ratio and dynamic range compared to conventional 3-T V-APS.

3.5 Layout

Figure 7 shows the layout of the test V-APS chip, including the proposed pixels, bias current sources and PGAs. PD is widely used vertically stacked on top of the TFT backplane [8]. Therefore, the PD is not shown in the layout.

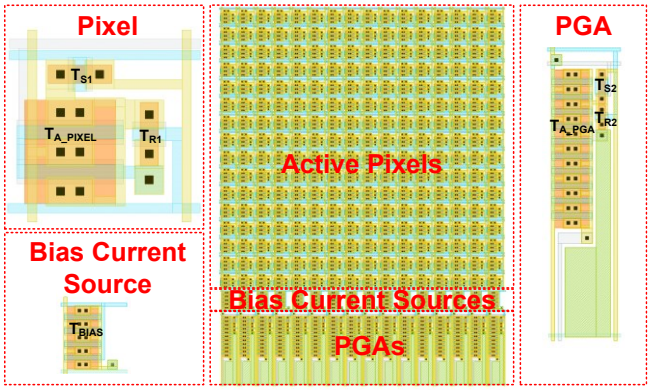

Figure 7. The layout of the proposed V-APS.

Table 1. Merits comparison among the proposed DG APS pixel and other related works.

	This Work	[4]	[5]	[3]
Technology	DG a-IGZO	LTPS	a-ITZO	a-IGZO
Critical dimension	6 μm	N/A	3 μm	3 μm
Operating principle	Voltage-mode	Voltage-mode	Voltage-mode	Current-mode
Pixel pitch	95 μm	50 μm	40 μm	100 μm
V_T compensation	√	×	×	×
Frame rate	30 Hz	N/A	10 Hz	50 Hz
Charge-to-voltage gain	**1.326 $\mu V/e^-$**	0.899 $\mu V/e^-$	0.131 $\mu V/e^-$	0.048 $\mu V/e^-$
Nonlinearity	**0.38%**	N/A	N/A	0.33%*

*After quadratic estimation

4. Conclusion

This paper proposes a high-gain voltage-mode active pixel sensor based on DG a-IGZO TFTs. This design enables both positive and negative V_T compensation. Furthermore, it employs a two-stage amplification structure to address the issue of insufficient gain in the in-pixel source follower configuration. The proposed circuit based on the 6 μm DG a-IGZO TFT technology, with a self-aligned structure to minimize parasitic capacitance, was demonstrated in terms of SPICE simulations, layout, and merits comparison. Research results show the CtV gain is 1.33 $\mu V/e^-$, with a nonlinearity of 0.38%. The output voltage error rate improves from 43.67% to 0.79% under a V_T shift of ±0.5 V. This work implements V_T compensation and programmable gain in a voltage-mode APS circuit. Moreover, compared to current-mode APS, this circuit significantly improves linearity and simplifies the structure of the ROIC, and is therefore promising for dynamic X-ray medical imaging applications.

5. Acknowledgements

This work was carried out at Guangdong Provincial Center for Oxide Semiconductor Devices and ICs, and supported financially by National Natural Science Foundation of China under Grant U24A20297, the Ministry of Science and Technology Key Research and Development Program under Grant 2022YFB3607200, Shenzhen Municipal Scientific Program under Grant JCYJ20220818100808019, and Xiaomi Innovation Foundation for University Program.

Email: zhangsd@pku.edu.cn

6. References

1. Karim K S, Nathan A. Readout circuit in active pixel sensors in amorphous silicon technology. IEEE Electron Device Letters, 2001, 22(10): 469-471.

2. De Roose F, Myny K, Steudel S, et al. 16.5 A flexible thin-film pixel array with a charge-to-current gain of 59μA/pC and 0.33% nonlinearity and a cost-effective readout circuit for large-area X-ray imaging. 2016 IEEE International Solid-State Circuits Conference (ISSCC). IEEE, 2016: 296-297.

3. El Gamal A, Eltoukhy H. CMOS image sensors. IEEE Circuits and Devices Magazine, 2005, 21(3): 6-20.

4. Tu C C, Wu S Y, Tai Y H. Comparison in the performance of passive and active TFT pixel sensing circuits using pin photodiode as the light sensing device. Digest of Technical Papers-SID International Symposium. 2021, 52(S1): 253-256.

5. Cheng M H, Zhao C, Huang C L, et al. Amorphous InSnZnO thin-film transistor voltage-mode active pixel sensor circuits for indirect X-ray imagers. IEEE Transactions on Electron Devices, 2016, 63(12): 4802-4810.

6. Izadi M H, Tousignant O, Mokam M F, et al. An a-Si active pixel sensor (APS) array for medical X-ray imaging. IEEE transactions on electron devices, 2010, 57(11): 3020-3026.

7. Zhang Y, Li J, Zhang Y, et al. Deep Sub-Micron Self-Aligned Bottom-Gate Amorphous InGaZnO Thin-Film Transistors with Low-Resistance Source/Drain. IEEE Electron Device Letters, 2023, 44(8): 1300-1303.

8. Cheng M H, Zhao C, Kanicki J. Study of current-mode active pixel sensor circuits using amorphous InSnZnO thin-film transistor for 50-μm pixel-pitch indirect x-ray imagers. Solid-State Electronics, 2017, 131: 53-64.