Advancing Electroluminescent Quantum-Dot LED (EL-QLED): Integration with CMOS Panels for Ultrasmall Displays in AR/VR Applications

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Abstract

The study focuses on developing quantum dot light-emitting diodes (QLEDs) with improved performance through optimized film quality and core/shell structures. A QLED with an external quantum efficiency (EQE) improved by approximately 44.8% and a high-brightness indium phosphide (InP) device with brightness of approximately 7,000 cd/m² were realized. A 0.08-inch CMOS integrated QLED microdisplay was demonstrated, which can be used for AR/VR microdisplays.

Author Keywords

Quantum-dots; QD-LED; CdSe; InP; ZnO; microdisplay; CMOS

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2. Objective and Background

QLEDs are at the forefront of next-generation display technology, offering outstanding color purity, tunable emission wavelengths, and high brightness. These features make them ideal for emerging smart displays, particularly in wearable AR/VR microdevices.

While cadmium selenide (CdSe) based quantum dots (QDs) have traditionally dominated due to their excellent electroluminescent performance, their toxicity has prompted a shift toward safer alternatives such as indium phosphide (InP) QDs. However, challenges remain in optimizing thin-film uniformity and carrier transport for both CdSe and InP QDs.

In response, this study is aimed at improving QLED performance and integrating them onto complementary metal-oxide-semiconductor (CMOS) backplanes, thereby laying a critical foundation for next-generation smart display technologies. With optimized film quality, ZnCdSeS QLEDs are fabricated, achieving a ~44.8% improvement in external quantum efficiency (EQE) and a brightness of 256,700 cd/m². For InP QLEDs, we fabricate devices achieving a brightness of ~7,000 cd/m² with proper QDs core/shell structures. Furthermore, we successfully integrate QLEDs onto CMOS backplanes, including the smallest known CMOS-integrated QD-microdisplay, with an active area of 1.5 × 1.5 mm² (0.08 inch). This work establishes a foundation for future high-resolution microdisplay advancements

3. Introduction

Quantum dot light-emitting diodes (QLEDs) represent a breakthrough in next-generation display technology, characterized by superior color purity, tunable emission wavelengths, and exceptional brightness. [1-3] .These attributes make QLEDs particularly attractive for emerging smart display applications, especially in wearable microdevices for augmented reality (AR) and virtual reality (VR). The combination of high color purity and cost-effective fabrication processes positions QLEDs as ideal candidates for these advanced applications. Among these, CMOS backplanes stand out due to their ability to offer independent pixel control, high driving currents, precise operation, and ultra-high resolution—advantages that surpass those of traditional thin-film transistor (TFT) backplanes—making them especially well-suited for microdisplays with pixel pitches below 10 μm. This synergy of QLEDs with CMOS backplanes underscores their potential as a leading solution for future high-precision microdisplay integration, paving the way for next-generation visual technologies.

Historically, CdSe QDs have dominated the QLED landscape due to their excellent electroluminescence (EL) performance and stability. However, the inherent toxicity of cadmium raises serious environmental and safety concerns, driving the exploration of alternative materials such as InP QDs, which are free from heavy metals and have emerged as a safer, more sustainable choice for QLEDs. Consequently, these two QD materials—CdSe and InP—represent highly promising candidates for integration with CMOS backplanes. Nevertheless, while both CdSe and InP QDs have demonstrated reliable performance in conventional device structures, significant challenges remain in controlling the carrier transport layer and ensuring the stability of coating solutions [4,5] —factors critical to successful CMOS substrate integration and major variables affecting performance.

In this study, we aim to improve and optimize QLED devices based on both ZnCdSeS and InP QDs for further backplane integration. For the ZnCdSeS QLEDs, devices with a ~44.8% improvement in EQE is fabricated. For InP QLED, device with a high maximum brightness (B_{max}) of ~7,000 cd/m² and a turn-on voltage (V_{on}) of ~2.5 V is also achieved. Finally, we successfully integrate QLEDs onto CMOS backplanes, realizing QD-microdisplays. By adopting a top-emitting structure and optimizing the microcavity effect, the world's smallest CMOS-integrated QD-microdisplay is developed, to the best of our knowledge, with a size of 1.5 × 1.5 mm² and a resolution of 1,663.8 pixels per inch (PPI). This breakthrough

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provides a sturdy foundation for the future advancement of high-resolution microdisplays

4. Experimental sections

Synthesis of Zinc oxide *(ZnO) Nanoparticles (NPs)*:

ZnO NPs were synthesized by dissolving 13.2 mmol of $Zn(OAc)_2 \cdot 2H_2O$ in 125 mL of methanol at room temperature. To this solution, 65 mL of KOH solution (0.5 M in methanol) was added under magnetic stirring at 60°C. The reaction was conducted under an argon (Ar) atmosphere for 1.5 hours. After the reaction, the product, a white precipitate, was purified using methanol. The precipitate was then re-dispersed in isopropyl alcohol (IPA), followed by the addition of dispersant ethanolamine (EA).

Fabrication of QD EL Device:

The QLED device structure consisted of ITO/ poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS)/ hybrid poly-N-vinylcarbazole (PVK) or hybrid poly(9,9-dioctylfluorenealt-N-(4-sec-butylphenyl)-diphenylamine) (TFB)/QDs/ZnO/Al. ITO glass substrates were cleaned sequentially with deionized water, isopropyl alcohol, acetone, and UV-ozone treatment. A thin film of PEDOT:PSS (filtered through a 0.45 μm filter) was spin-coated onto the substrates at 3000 rpm. Following this, PVK (7.5 mg/mL) and TFB (2.5 mg/mL) solutions were prepared under the same spin-coating conditions to form the hole transport layer (HTL). The quantum dot emitting layer was prepared by dissolving the QDs (30 mg/mL ZnCdSeS and 10 mg/mL InP QDs in octane). The electron transport layer (ETL) was formed by spin-coating a ZnO NP solution (30 mg/mL in isopropyl alcohol) at 5000 rpm, followed by baking at 100°C for 10 minutes. Finally, the devices were completed by evaporating an aluminum (Al) or silver (Ag) layer as the top electrode.

5. Results

Optimization of Standard QLEDs: In this study, ZnO NPs are employed as the electron transport layer (ETL) for both ZnCdSeS and InP QLEDs. The ZnO NPs are synthesized following previously reported methods [6,7] . To improve the carrier recombination, EA was introduced as dispersant. To confirm ZnO dispersion quality and particle size, dynamic light scattering (DLS) analysis was performed, revealing a well-dispersed state with an average particle size of approximately 13 nm.

Table 1 presents the core/shell structures of the ZnCdSeS and InP quantum dots (QDs) utilized in this work, highlighting their compositional and structural properties. Table 2 summarizes the carrier mobility of the optimized QLED devices. The carrier mobilities of different QDs are calculated using the Mott-Gurney equation based on measurements from fabricated single-carrier devices [8] . where μ is the effective carrier mobility at the space charge limit current region, ε is the permittivity ($\varepsilon_{PVK} = 2.1 \times 10^{-11}$ F m^{-1}, $\varepsilon_{TFB} = 3.1 \times 10^{-11}$ F m^{-1}), [9-11] V is the applied voltage, and d is the film thickness.

$$J_{SCLC} = \frac{9}{8}\mu_{SCLC}\varepsilon\frac{V^2}{d^3} \qquad (1)$$

Devices are fabricated with the typical structure ITO/PEDOT:PSS/PVK/ZnCdSeS QDs/ZnO/Ag and ITO/PEDOT:PSS/TFB/InP QDs/ZnO/Al respectively. For the ZnCdSeS QLEDs, with adjustment of ZnO solution dispersion , device optimization enhances the external quantum efficiency (EQE) from 5.8% to 8.4% (a 44.8% improvement) and increases the maximum brightness to 256,700 cd/m², achieving high-luminance performance. For the InP QLEDs, the core/shell structure of QDs is found that with the thicker ZnSe shell of ~4.8 nm, the improved devices exhibited a maximum brightness of approximately 7,000 cd/m² and a turn-on voltage of about 2.5 V. These findings demonstrate the effectiveness of the device structures and the potential for further optimization. The device performance is shown in Figure 1 .

Table 1. Properties of QDs with different core/shell/shell structures

	ZnCdSeS QDs	InP QDs
Core	11.3 nm (ZnCdSeS Alloyed Core)	3.4 nm (InP Core)
1st Shell	2.6 nm (ZnS)	4.8 nm (ZnSe)
2nd Shell	--	1.3 nm (ZnS)
PL Peak	524 nm	618 nm

Table 2. Carrier mobility of devices fabricated with ZnCdSeS and InP QDs

	ZnCdSeS QLEDs	InP QLEDs
Hole mobility ($cm^2 V^{-1} s^{-1}$)	1.1×10^{-8}	1.1×10^{-4}
Electron mobility ($cm^2 V^{-1} s^{-1}$)	1.3×10^{-4}	2.1×10^{-4}

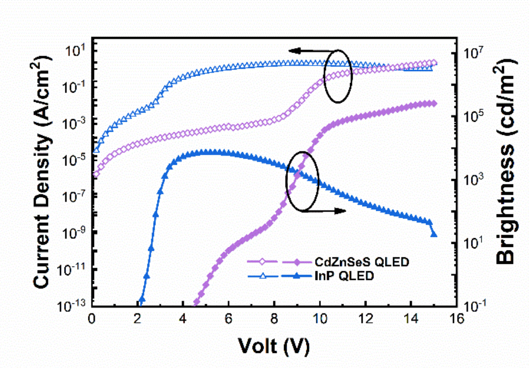

Figure 1. J–V–B characteristics of ZnCdSeS- and InP-based QLEDs.

CMOS Integrated QD-microdisplay: Figure 2(a) shows an integrated InP QLED device in the CMOS backplane (chip area 4.5 x 4.5 mm²). The direct integration process of QLED device layers into CMOS backplane by spin-coating appears to be workable. By this approach, device layers are spin-coated on all the backplane substrate, where the active area is located at the central part of the backplane chip. Note that the CMOS backplane is loaded on a circuit board used to connect to an external power supply. The array area of the chip is 1.5 x 1.5 mm², which contains an array of 8-μm Al electrodes, as shown in Figure 2(b). To integrate QLEDs on the CMOS backplane, all the device layers, such as injection layers, carrier transport layers, and QD layers, are sequentially coated on the backplane substrate by a spin-coater. As current spin-coating of QDs is directly carried out on the circuit board rather than a smooth glass substrate, the spin-coating process is challenging because the surface of the circuit board is not a smooth surface. Spin-coating of materials is carried out by directly dispensing InP precursor solutions of the device layers on the backplane for spin-coating process. It appears that the reproducibility of QLED emission is low, attributed to relatively low dispersion of InP QDs in octane. This will be further improved by ligand exchange in the near future. Figure 2(c) shows the integration of ZnCdSeS QLEDs in the same type of CMOS substrate, as shown in Figure 2(c). The ZnCdSeS QD precursor solution has relatively better dispersion and the coated film appears to be more uniform. Electroluminescence can be observed with the naked eye. The green-light-emitting area comprises 100 × 100 individual pixels, each corresponding to an Al electrode mentioned earlier. The resolution of this 0.08-inch QD microdisplay is calculated to be 1663.8 pixels per inch (PPI) within a 1.5 × 1.5 mm² array area, which represents the world's smallest QD microdisplay to the best of our knowledge. This breakthrough demonstrates an advancement in smart display technology and establishes a robust foundation for the future development of high-resolution microdisplays.

In the context of smart display technologies, taking AR glasses as an example, the display principle is similar to projecting the image onto an optical lens, which is then transmitted to the human eye through a waveguide lens. Traditionally, larger display sizes have led to discomfort for users due to the bulkiness of the wearable device. However, the small-size QD-microdisplay developed in this study significantly reduces the display module size and is expected to effectively overcome the limitations of traditional displays in future AR applications. This technology not only enhances the portability of the device but also offers a more adaptable and innovative solution for future display technologies, showcasing the broad potential of display modules in AR/VR fields.

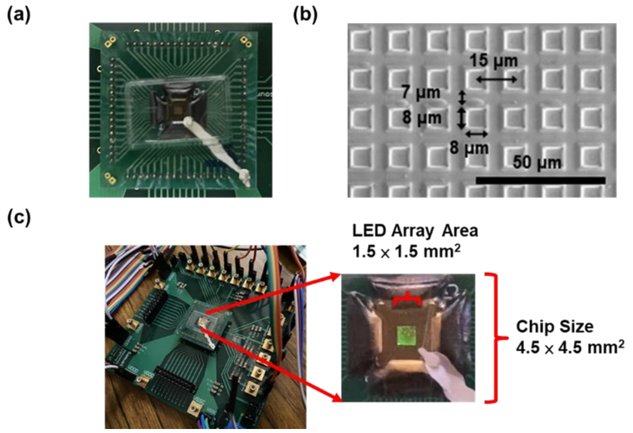

Figure 2. Integration of QLEDs with 4.5 x 4.5 mm² CMOS backplane. **(a)** Photograph of InP QLED integrated in CMOS backplane. **(b)** Scanning electron microscope (SEM) bird-view image of the 0.08-inch CMOS backplane. **(c)** Photograph of ZnCdSeS CMOS QLED integrated in CMOS backplane. The CMOS backplane features a device size of 1.5 × 1.5 mm² (0.08 inch).

6. Conclusion

This study introduces a 0.08-inch CMOS-integrated EL-QLED microdisplay with a resolution of 1663.8 PPI and a pixel pitch of 15 µm, representing a significant advancement in high-resolution mobile display technology. The findings highlight the feasibility of fabricating ultra-small displays using a wet-coating process for QDs and lay the groundwork for future innovations in stable, high-performance QLED devices and smart display applications.

7. Impact

In this study, we improve the device performance through optimized film quality and core/shell structure of ZnCdSeS and InP QDs for developing CMOS QD-microdisplay. We successfully integrate QLEDs onto 0.08-inch CMOS backplanes, achieving what we believe to be the world's smallest CMOS QD-microdisplay. These results provide a reliable foundation for the future development of smart displays, offering improved stability and performance for advanced optoelectronic applications.

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