

Photolithography-Based Micropatterning Integration of Quantum-Dot Electroluminescent Displays with Nonvolatile Charge Trap Memory

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Abstract

A memory-in-pixel (MIP) is demonstrated using non-volatile charge trap memory with an Al₂O₃/HfO₂/Al₂O₃ (AHA) structure and integrated quantum dot light-emitting diodes (QD-LED). The AHA structure exhibits high charge trapping capacity, achieving a 4.7 V memory window, Ion/off ratio of 10⁸. The integration of QD-LED enables a self-erasing functionality via the photovoltaic effect without an external light source.

Author Keywords

Charge Trap Thin-Film Transistor (CTTFT); Quantum Dot Light-Emitting Diodes (QD-LED); Monolithic integration; High-Resolution Display

1. Introduction

The growing demand for augmented reality (AR) and virtual reality (VR) is leading to rapid advancements in display technologies to achieve ultra-high resolution over 3,000 pixels per inch (PPI). Organic light-emitting diodes (OLED) – on – Silicon devices, commonly used in AR and VR displays, rely on white OLED emitters combined with color filters. However, this approach faces significant challenges, including low power efficiency, limited resolution, and high manufacturing costs, which hinder commercialization. To achieve the requirements for ultra-high resolution, it is essential to reduce pixel sizes in the front plane while maintaining compatibility with established semiconductor manufacturing process, such as photolithography. In display backplane side, fast-response devices and smaller transistors are necessary to drive compact pixels efficiently while preserving the aperture ratio of emissive display elements^[1].

Conventional active matrix (AM) displays face scaling challenges due to their dependence on capacitors for charge storage. As the sub-pixel area decreases and transistor counts increase, the area-dependent nature of capacitance limits the scalability of these components^[2,3]. To solve the aforementioned problems, memory-in-pixel (MIP) technology introduces non-volatile memory to replace storage capacitors^[4-6]. By reducing the number of components per pixel, this approach increases the aperture ratio and simplifies the structure, allowing stable image maintenance without frequent refresh cycles. These advancements improve power efficiency, extend panel life time and support the development of ultra-high resolution, high-density displays.

In this study, we propose a MIP device fabricated by combining a quantum dot light-emitting diodes (QD-LED) with charge trap-based nonvolatile memory transistors using a photolithography-based lift-off process. The charge trap thin film transistor (CTTFT) serves as a memory cell that supports high-performance displays by providing high data retention, low power consumption, and excellent durability. However, oxide semiconductors, which are used as the channel layer in CTTFT,

typically generally exhibit n-type characteristics to make it difficult to erase data by conventional de-trapping methods. To solve this problem, we implemented an independent data-erasure function without requiring additional devices by utilizing the photoelectric effect that utilizes the light source generated inside the QD-LED device. The QD-LED serves both as a front-plane light emitter and as a photon source for the CTTFT, enabling the memory's charge to be self-erased without external components. By overcoming the limitations of micro-LEDs and OLEDs, the integrated QD-LED and CTTFT system offers a scalable solution for next-generation AR/VR displays.

2. Results and discussion

2.1 CTTFT characteristics using AHA structure

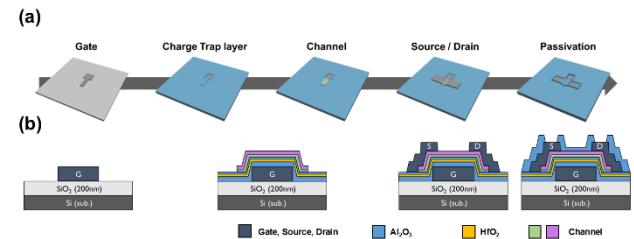


Figure 1. Schematic of CTTFT fabrication process, a) 3D image of CTTFT device top view, b) cross-sectional view of CTTFT device.

To implement MIP technology, a charge trapping layer with an Al₂O₃ / HfO₂ / Al₂O₃ (AHA) structure was employed. The AHA structure exhibits superior charge trapping capacity and stability compared to the Si₃N₄ structure^[7,8]. HfO₂ is widely studied high-k dielectric materials known for its trap-rich properties, making it an excellent choice for charge trapping memories. Its high dielectric constant allows it to trap charges more effectively enabling a wider memory window, for example, a 2 nm HfO₂ layer has a better charge trapping performance than 7 nm Si₃N₄. The Al₂O₃ layers reduce leakage currents and enhancing overall stability and data retention^[9-11]. The CTTFTs were fabricated using the process shown in Figure 1.

Figure 2a shows the high-frequency (1 MHz) capacitance – voltage (C-V) curves for the metal-AHA-semiconductor-metal structure. The devices showed counterclockwise hysteresis in C-V curves when the gate voltage is swept from -10 V to 10 V, which means that the successful charge trapping of AHA structure. A CTTFT device utilizing the AHA structure achieved a maximum memory window (MW) of 4.7 V, and a high Ion/off ratio of over 10⁸ (Figure 2b).

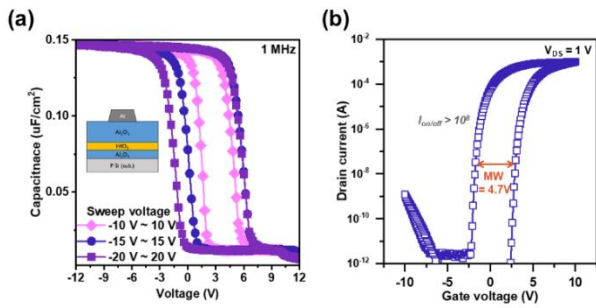


Figure 2. Characterization of CTTFT. a) C-V characteristics of AHA structure, b) transfer characteristics of CTTFT at $V_{DS} = 1$ V.

2.2 Erasing mechanism of CTTFT with QD-LED

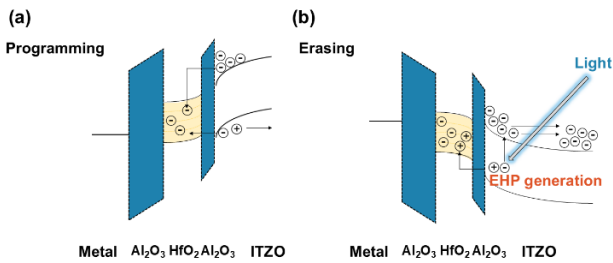


Figure 3. Schematic energy band diagram of the CTTFT and QD-LED a) Programming mechanism, and b) erasing mechanism.

During the programming process, a positive gate voltage causes electron trapped in the charge trapping layer (Figure 3a). In conventional floating-gate memories, a de-trapping mechanism involving hole injection with negative bias was utilized due to damage from repeated erasing cycles. However, the oxide semiconductors, such as amorphous indium tin zinc oxide (a-ITZO) and amorphous indium gallium oxide (a-IGZO), present challenges for hole transport due to localized valence band maximums^[12]. The holes generated from electron-hole pairs by the photovoltaic effect recombine with the trapped electrons in the charge trapping layer, effectively removing the trapped electrons (Figure 3b).

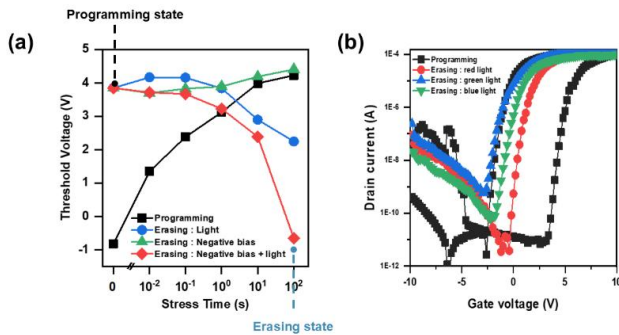


Figure 4. Programming / erasing characteristics of CTTFT a) under different stress times and erasing test with various methods, b) under various wavelength illumination.

To investigate the mechanism of the erasing process, we performed erasing tests using three different methods, as shown in Figure 4a. First, we applied external light alone, which resulted in a slight shift in V_{th} compared to the programmed state. Second, we applied a negative bias only, which showed no significant change in V_{th} . Finally, we applied both external light and a negative bias together, successfully restoring V_{th} to its initial state. Additionally, the erasing process can be controlled by adjusting the wavelength of the applied light, demonstrating its potential for use in display applications (Figure 4b).

2.3 Fabricated of integrated CTTFT and QD-LED

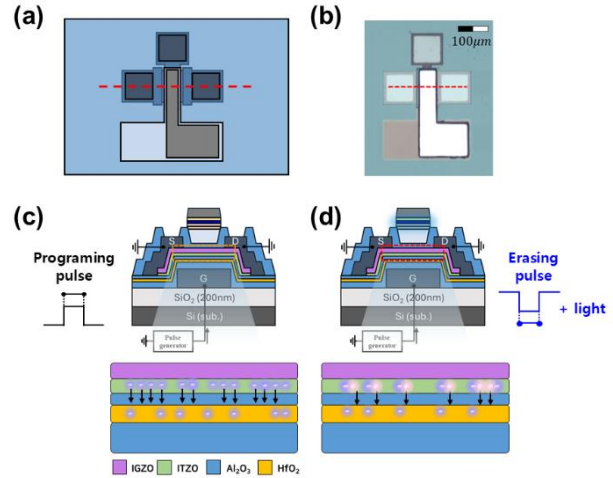


Figure 5. a) Schematic of the integrated CTTFT and QD-LED device (top view), b) top view of integrated device, c) cross-sectional schematic of the integrated device during the programming pulse process, and d) cross-sectional schematic of the integrated device during the erasing pulse process with QD-LED light.

Further improvements included integrating a QD-LED as an internal light source, eliminating dependence on external lighting. Unlike micro-LEDs, which face challenges in epitaxy growth in sapphire substrate and transfer process^[13], and OLEDs, which face challenges of solution process and processing in atmosphere condition. QD-LEDs offer a wide color gamut and compatibility with solution process^[14,15], making them particularly suited for monolithic integration. The result is a device capable of independent program/erase operations and demonstrating potential for advanced MIP.

The MIP device is fabricated with QD-LED through a lift-off process that employs photolithography. This method can remove unwanted QD-LED layers deposited on the photoresist. The demonstration of the integrated devices of CTTFT and QD-LED was illustrated in Figure 5a. Figure 5b showed the optical microscope (OM) image of the integrated region of the CTTFT and QD-LED, demonstrating the successful implementation of the monolithic process. Figure 5c illustrates a schematic of the self-programming process in a device integrated a CTTFT and QD-LED, where electrons are trapped in the charge trapping layer under a positive bias. When the QD-LED emission in the integrated device, light generates electron-hole pairs in the channel layer, where holes are transported to HfO₂ under a negative bias, enabling charge erasing. As a result, integrating

QD-LED into the CTTFT system eliminates the need for an external light source and enabling the implementation of a self-programming/erasing device.

3. Conclusion

We demonstrate successful monolithic integration of a QD-LED with a CTTFT, enabling effective memory erase functionality for MIP technology. By utilizing QD-LED as internal light sources to facilitate charge de-trapping in non-volatile memory, this approach simplifies device structures reduces power consumption and enhances efficiency. Unlike conventional oxide-based memory relying on external light sources, QD-LED emission generates sufficient electron-hole pairs for trapped charge recombination. Tailoring the QD-LED emission and channel layer bandgap alignment optimizes memory erase performance, enabling pixel level reprogramming and localized erasure.

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