LTPS-TFT-Based Scan Driver Circuit with Stable Dual-Polarity Outputs by Bootstrapping Without Pre-Charging

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Abstract

We propose a scan driver circuit based on p-type low-temperature polycrystalline silicon thin-film transistors (TFTs) capable of stable dual polarity outputs. A novel method of bootstrapping the gate node of pull-down TFTs directly without a pre-charging period is used for ripple-free outputs.

Author Keywords

Scan driver circuit; dual polarity outputs; ripple-free; bootstrapping without pre-charging; p-type low-temperature polycrystalline silicon thin-film transistor

1. Introduction

Active-matrix organic light-emitting diode (AMOLED) displays have been widely used in the display industry because of their large-color gamut, wide-viewing angle, high contrast ratio, vivid colors, and low power consumption [1], [2]. AMOLED displays are mainly designed with pixel circuits that require scan signals with dual polarity. Therefore, a scan driver circuit capable of two dual polarity outputs with only one control part has the advantages of being applicable for high resolution and narrow bezel displays [3]. Moreover, the scan drivers based on low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) can further reduce circuit area because of their excellent current-driving capabilities [4], [5].

However, p-type LTPS TFTs-based scan driver circuits have one issue to be solved for stable outputs. Because of the characteristics of p-type TFTs [6], [7], the gate node of pull-down TFTs (QB[n]) must be periodically bootstrapped to maintain a low-level voltage (VSS), during the off-state period, as shown in Figure 1(a). Then, the gate node of pull-up TFT (Q[n]) is charged to VDD, and QB[n] is bootstrapped simultaneously. Therefore, since the pull-up TFT and pull-down TFT are turned on momentarily at the same time, a ripple of QB[n]–V_{TH} (threshold voltage) occurs, as shown in Figure 1(b).

This unstable output with the ripple cause voltage distortion when applying data voltage to pixel circuits, making accurate gray level expression difficult. Controlling the duties of the clock signals can be a solution to this issue by moving the bootstrapping timing. However, this method not only requires additional clock signals, but also reduces the pulse width of scan signals, thus the data voltage is not sufficiently applied to the pixel circuit. Therefore, a new concept for stable dual polarity outputs without ripples should be proposed.

In this study, we propose a p-type LTPS TFTs-based scan driver circuit with stable dual polarity outputs. The proposed circuit could eliminate ripples by directly bootstrapping QB[n] without the pre-charging period, thereby discharging QB[n] to a voltage lower than VSS before Q[n] is charged to VDD. We demonstrated that the proposed circuit successfully eliminated the ripples through simulation and measurement results.

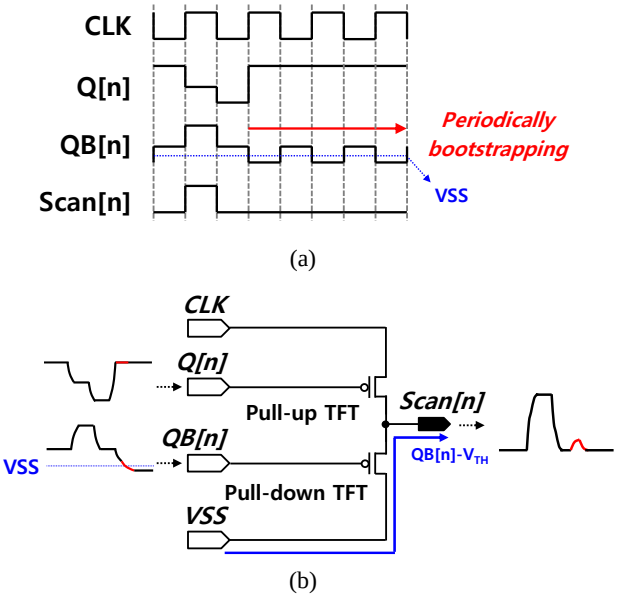

Figure 1. (a) Periodically bootstrapping the gate node of pull-down TFT (QB[n]) for stable off-state operation and (b) ripple using the conventional bootstrapping method.

2. Proposed Scan Driver Circuit

Figure 2 shows the circuit schematic and timing diagram of the proposed scan driver circuit capable of high- and low-level dual polarity output (HLDO) signals without ripples. The proposed circuit consists of ten p-type LTPS TFTs and three capacitors with two clock signals and two DC signals (VDD, VSS). The circuit eliminated ripples by adding only one capacitor (C3) without additional clock signals. Moreover, stable operation is possible because the bootstrapping of the gate node of pull-down TFT (T2) by C3 is done with the DC signals (VSS) rather than AC (clock) signals. The operation process is divided into four periods: (1) Scan[n] output, (2) Scanb[n+1] output, (3) reset and hold I, and (4) hold II.

During the Scan[n] output period, when Scanb[n] is discharged to VSS, QB1[n] is charged to VDD through T10 and turns off T2. Thus, Scan[n] generates a high-level voltage output through T1. Because Q[n] is discharged to VSS–V_{TH} through T3, Scanb[n+1] maintains a high-level voltage output.

During the Scanb[n+1] output period, as Scanb[n] and CLK switch to VDD and VSS, respectively, T1 is turned off, QB1[n] is discharged through T8, and T2 is turned on. When Scan[n] is discharged through T2, the voltage of QB1[n] decreases due to the coupling effect of C3. Then, as the gate-to-source voltage (V_{GS}) of T8 becomes higher than V_{TH}, T8 is turned off and QB1[n] becomes floating. Thus, QB1[n] is bootstrapped to a voltage

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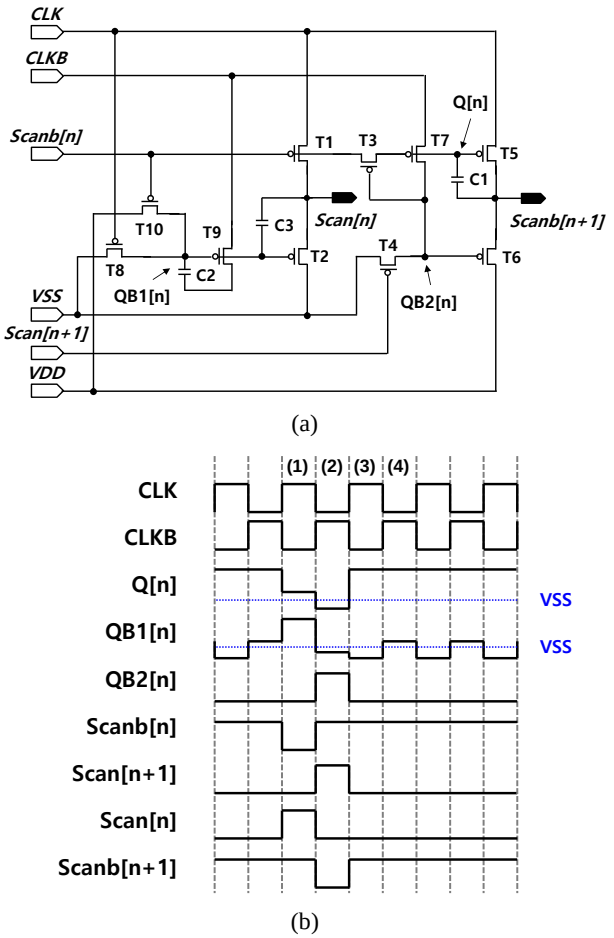


Figure 2. Proposed scan driver circuit: (a) circuit schematic and (b) timing diagram.

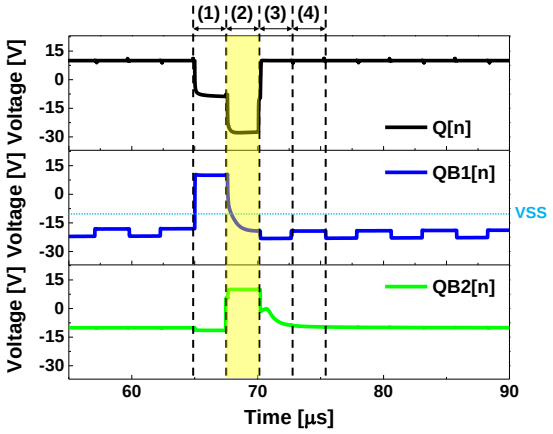


Figure 3. Simulated voltage waveforms of Q[n], QB1[n], and QB2[n].

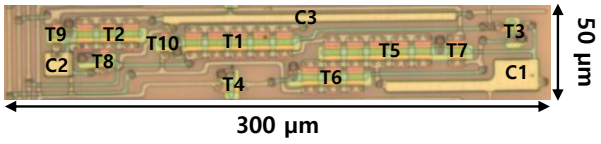


Figure 4. Microscope image of the fabricated scan driver circuit.

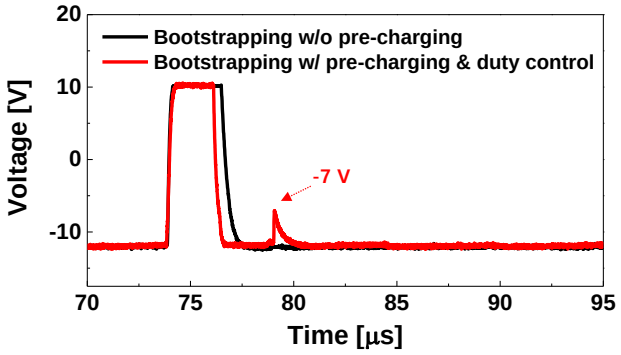
lower than VSS. Therefore, Scan[n] can be discharged directly to VSS, not VSS–V_{TH}. Also, as Q[n] is bootstrapped, Scanb[n+1] generates VSS through T5.

During the reset and hold I period, as CLKB switches to VSS, QB1[n] is bootstrapped. Since QB1[n] was already at a voltage lower than VSS by bootstrapping without the pre-charging period, Scan[n] can generate a stable low-level voltage output without the ripples. Then, when Q[n] is charged to VDD by Scanb[n] through T3, T5 and T7 are turned off. Because QB2[n] is discharged to VSS through T4, Scanb[n+1] generates high-level voltage output through T6.

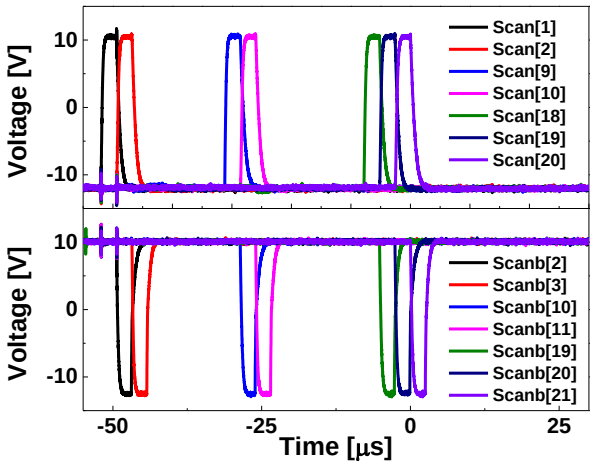
During the hold II period, as QB1[n] and QB2[n] have low-level voltage, Scan[n] and Scanb[n+1] maintain low-level voltage output and high-level voltage output through T2 and T6, respectively.

3. Results and Discussion

We investigated the circuit operations using simulation tools (SmartSpice, Silvaco). Scan[n] and Scanb[n+1] swing in the range of -12 V (VSS) to 10 V (VDD). Figure 3 indicates the simulated voltage waveforms of Q[n], QB1[n], and QB2[n]. During the Scanb[n+1] output period, QB1[n] was directly bootstrapped by the coupling effect of C3. Therefore, since QB1[n] continued to maintain a voltage lower than VSS, Scan[n] could stably generate VSS in off-state operation.



(a)



(b)

Figure 5. (a) Comparison of Scan[n] using the bootstrapping method with and without pre-charging and (b) measured output voltage waveforms of the fabricated scan driver circuit.

Figure 4 shows an optical image of the fabricated scan driver circuit. The fabricated circuit area was 50 × 300 μm^2. The proposed circuit could effectively decrease the circuit area by adding only C3 of 0.08 pF without additional clock signals.

We verified the ripple-free operation by measurements. Figure 5(a) exhibits the comparison of measured Scan[n] between the circuit using the conventional bootstrapping method with the pre-charging and the circuit using the proposed bootstrapping method without the pre-charging. The output of the circuit using the conventional bootstrapping method had a ripple of about -7 V even though the duties of the clock signals were controlled to improve the ripples. However, the proposed scan driver circuit successfully generated a high-level voltage output with a longer pulse width and no ripple by bootstrapping QB1[n] without the pre-charging period.

Figure 5(b) shows that the fabricated circuit successfully generated Scan[n] and Scanb[n+1]. Moreover, since QB1[n] and QB2[n] were continuously maintained at a low-level voltage, Scan[n] and Scanb[n+1] maintained stable off-state voltages. Consequently, the measurement results verify the ripple elimination operation of the proposed scan driver circuit.

4. Conclusion

We proposed a p-type LTPS TFTs-based scan driver circuit capable of stable HLDO signals without ripples. The elimination of the ripples was possible by bootstrapping QB1[n] to the voltage lower than VSS without the pre-charging period. The simulation results confirmed that QB1[n] was directly bootstrapped by the coupling effect of C3 during the Scanb[n+1] output period. Moreover, the proposed circuit effectively reduced the circuit area by adding only one capacitor without additional duty-controlled clock signals. The fabricated circuit successfully generated Scan[n] and Scanb[n+1] without ripples. Consequently, we demonstrated the stable operation of the proposed scan driver circuit.

5. Acknowledgements

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