High Performance, Flexible Ferroelectric Thin Film Transistor on PI Substrate

Samiran Roy[1,2], Jewel kumer Saha[1,3], Junmi Lee[1], Heonbang Lee[1], and Jin Jang[1]*

[1]Advanced Display Research Center and Department of Information Display Kyung Hee University, Seoul 130-701, Korea, [2]Department of Physics, University Barishal, Barishal-8254, Bangladesh, [3]Department of Physics, Jagannath University, Dhaka-1100, Bangladesh

Abstract

We present flexible ferroelectric HZO TFTs on polyimide (PI) substrate, with a nanocrystalline IGZO active semiconductor. The TFTs exhibit stabilized ferroelectricity at 350 °C, anti-clockwise hysteresis with memory window (MW) of ~5 V, subthreshold swing (SS) of 120 mV/decade, and I_{ON}/I_{OFF} ratio of ~8.9×10^6. The MW of the flexible FE-TFTs changes a little upon mechanical bending strain (MBS) of 0.32% at 2 mm radius.

Keywords

Ferroelectric HZO, flexible PI substrate, spray pyrolysis, mechanical flexibility.

1. Introduction

Flexible electronics have garnered significant interest in today's energy-conscious world for their bendability, lightweight design, and user-friendly interfaces. [1] To enable next-generation technologies, flexible active elements are essential for memory applications and ultra-edge computing. The ferroelectric (FE) hafnium zirconium oxide (HZO) thin film transistor (TFT) on flexible substrates have emerged as promising candidates for non-volatile memory (NVM) and synaptic devices. [2] This advancement is driven by exceptional properties of hafnia-based materials, including complementary metal oxide (CMOS) compatibility, high remnant polarization, high coercive field, energy efficiency, low annealing temperature and ultra-thin scaling. Ferroelectricity in HfO_2-based films arises from the formation of a polar orthorhombic phase ($Pca2_1$). This phase transition can be induced by reducing grain size, adding dopants like Zr, La, Y, Al, Gd, and Sr, applying biaxial stress, or introducing point defects. Extensive research on these materials has enabled applications in non-volatile memory, neuromorphic devices, displays, and energy harvesting. [3-4]

FE-TFTs typically require high fabrication temperatures, making them less suitable for flexible substrates and limiting their application in wearable devices. However, HZO's annealing temperature has been reported to align with back-end-of-line (BEOL) processing conditions. Consequently, significant efforts have been directed toward the development of HZO FE-TFTs on polyimide (PI) substrates due to their superior flexibility, durability, thermal stability, lightweight and compatible with BOEL process temperature. [5] Sputtering, atomic layer deposition (ALD), and pulsed laser deposition (PLD) are well-established deposition techniques for ferroelectric HZO thin films. However, there is a growing preference for solution-based methods like spray-coating, owing to their potential for low cost, environmental stability, large-area uniformity, and the ability to induce ferroelectricity in thicker films. [6-9]

In this study, we present the inverted staggered, flexible HZO FE-TFTs on PI substrate with a nanocrystalline indium gallium zinc oxide (IGZO) active layer and HZO gate insulator (GI) layer, utilizing a low-cost spray pyrolysis system. The ferroelectricity in the HZO layer, stabilized at 350 °C, improved with a thin ZrO_2 seed layer, is verified through grazing incidence X-ray diffraction (GI-XRD), capacitance, and polarization measurements. The transfer characteristics of the HZO TFTs on PI show anti-clockwise hysteresis with a memory window (MW) of ~5 V, a low subthreshold swing (SS) of 120 mV/decade, and an I_{ON}/I_{OFF} ratio of ~8×10^6, confirming the ferroelectric nature of the GI. The devices maintain robust electrical performance under mechanical bending strain (MBS) with bending radius ranging from flat to 2 mm. Notably, a negligible MW degradation was observed after MBS of 0.32% at a 2 mm bending radius.

2. Experimental details

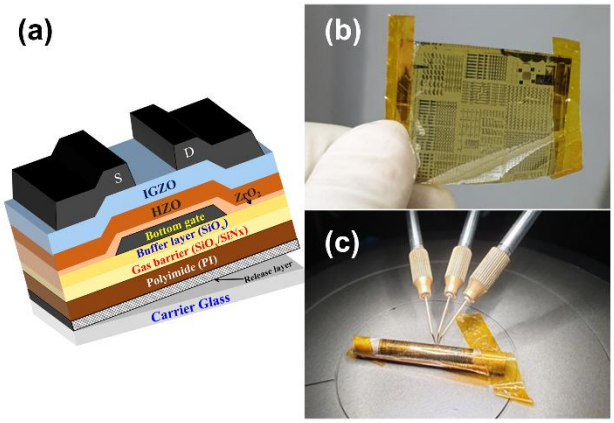

Figure 1. (a) Schematic cross section of FE-TFT on PI substrate. (b) The flexible FE-TFTs on PI after mechanical detachment. (c) Image of the flexible FE-TFTs being rolled to a cylinder of a radius of 3 mm.

Fig. 1(a). shows the schematic structure of an inverted staggered HZO FE-TFT on PI substrate. The FE-TFT fabrication process proceeds as follows: A thin CNT layer is deposited via spray pyrolysis at 100 °C, enabling easy mechanical detachment [10]. A 10 μm thick PI substrate is then spin-coated onto the CNT layer and annealed for 2 h in an N_2 chamber. Next, a 125 nm gas barrier layer comprising alternating SiN_x/SiO_x layers (25 nm each) is

ISSN 0097-996X/25/5603-2052-$1.00 © 2025

deposited with a buffer layer of 300 nm SiO_2 on it. An 80 nm thick molybdenum (Mo) layer is subsequently deposited and patterned to form the bottom gate electrode. The process continues with the sequential deposition of a ZrO_2 layer (~10 nm thick) and a FE HZO layer (~30 nm thick) by spray pyrolysis at 350 °C. The HZO solution was synthesized in an N_2 glovebox environment using zirconium (IV) 2,4-pentanedionate ($C_{20}H_{28}O_8Zr$) and hafnium isopropoxide isopropanol ($C_{12}H_{28}HfO_4$) as zirconium and hafnium precursor and 2-methoxyethanol (2-ME) as solvent. Similarly, ZrO_2 solution also prepared in 2-ME with ($C_{20}H_{28}O_8Zr$) for seed layer. A 5 nm nanocrystalline IGZO channel layer is then deposited via spray pyrolysis at 425 °C. The IGZO solution was synthesized in a nitrogen glovebox using indium chloride ($InCl_3$), gallium (III) nitrate hydrate ($Ga(NO_3)_3 \cdot xH_2O$,) and Zinc acetate dihydrate ($C_4H_{10}O_6Zn$) as precursors for indium, gallium, and zinc, respectively and 2-ME as solvent. The c-IGZO and FE GI are patterned to have the active island and contact holes, respectively. For the source and drain (S/D) electrodes, an 80 nm Mo layer is deposited and patterned, followed by post-fabrication annealing at 250 °C for 2 hrs. Fig. 1(c-d) illustrate the photographic image of the fabricated TFT array on a 10 µm PI substrate, as well as the mechanical strain observed on cylindrical structure.

All electrical measurements were performed by the Agilent 4156 C semiconductor parameter analyzer in the dark at room temperature. The threshold voltage (V_{TH}) was defined as the V_{GS} corresponding to I_{DS}=W/L x10 pA. The memory window (MW) was calculated as the difference between the two distinct V_{TH} values at forward and reverse bias on the transfer curve, corresponding to an I_{DS} of 10 nA. The TFT width (W) and length were defined as the difference between the source and drain area. The subthreshold swing (SS) is taken as ($d\log(I_{DS})/dV_{GS}$)-1 of the range 10 nA ≤ I_{DS} ≤ 100nA, with V_{DS} = 0.1

3. Results and Discussion

Fig. 2(a) illustrates the GI-XRD spectra of the ZrO_2/HZO thin film, revealing a distinct diffraction peak at a 2θ angle of ~30.40°, identified as the non-centrosymmetric orthorhombic phase. Fig. 2(b) presents an HR-TEM image (magnified view) of the HZO layer, showing its polymorphic crystalline structure. The inset displays the measured FFT peaks, assigned to the (111), (21$\bar{1}$), and (10$\bar{2}$) planes of the orthorhombic structure. The measured capacitance-voltage (C–V) characteristic of the MFM capacitor, shown in Fig. 2(c), demonstrates hysteresis with a bowknot-like feature, confirming the ferroelectricity within the GI layer. Fig. 2(d) shows the P–V curve of the ZrO_2/HZO-based MFM device, which exhibits significant hysteresis with a rounded shape and a 2Pr value of 14.52 µC/cm².

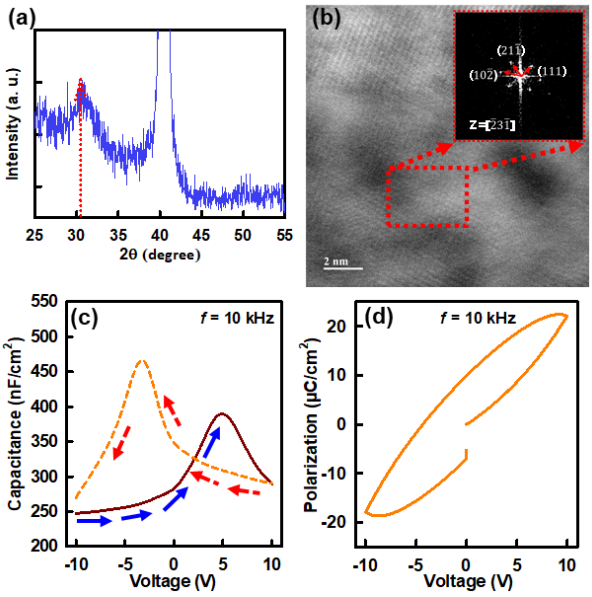

Figure 2. (a) GI-XRD spectra of ZrO_2/HZO on Mo substrate deposited at 350 °C. (b) HR-TEM image of the ferroelectric HZO layer, inset showing the FFT of the selected area marked by red rectangles. (c) Capacitance–voltage and (d) Polarization-voltage characteristics from the MFM structure measured at a frequency of 10 KHz.

Fig. 3(a) displays a microscopic photograph of the flexible FE-TFT, with a channel width (W) of 50 µm and length (L) of 10 µm. The C–V characteristics measured for the metal–insulator–semiconductor (MIS) structure (Fig. 3(b)) reveals a memory window (MW), defined as the flat band shift width induced by the ferroelectric field effect, of 4.1V. Fig. 3(c) illustrates the transfer curves with anti-clockwise hysteresis measured in double-sweep mode starting from -6V to +6 V then to -6 V with V_{DS} of 0.1 V. we changed the sweeping voltages to ± 8 V, and up to ±10 V. The MW of the FE-TFT increases with V_{GS}, demonstrating tunability, with an MW of ~5 V, a low subthreshold swing (SS) of ~120 mV/dec, and a high I_{ON}/I_{OFF} ratio of ~8.4 × 10^6 at V_{GS} of ±10 V. This behavior aligns with the ferroelectricity observed in the flexible FE-TFT making it suitable for memory and synaptic applications. The gate leakage current (I_{GS}), shown in Fig. 3(d), exhibits a distinct current peak, further confirming the ferroelectric nature of the HZO layer.

To evaluate flexibility of the ferroelectric HZO FE-TFT, the devices were tested in both the flat state and under bending radii of 10, 7, 5, 3, and 2 mm at room temperature and atmospheric conditions. It is important to note that the device was positioned at the center of the flexible substrate during the bending tests. Fig. 4(a) and (b) exhibit the I_{DS} vs V_{GS} and I_{GS} vs V_{GS} characteristics with anticlockwise hysteresis of flexible HZO FE-TFTs under different tensile stress, respectively. The I_{DS} vs V_{GS} curves exhibit the minimal change of MW of about 0.5 V

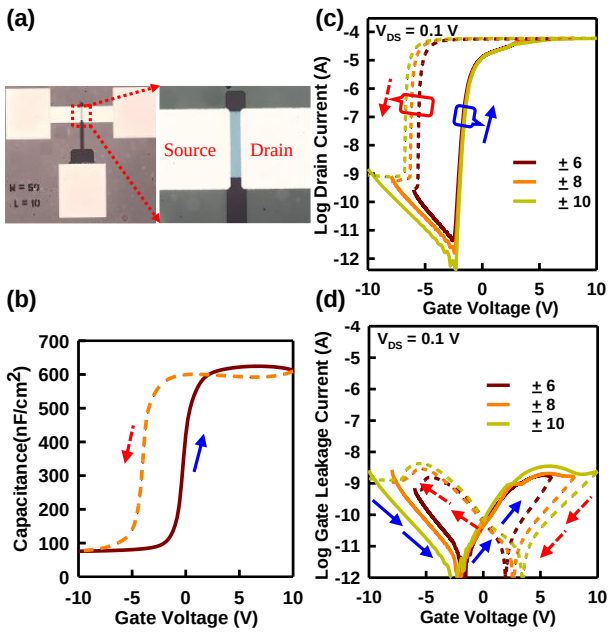

Figure 3. (a) Optical microscopy image of a flexible FE-TFT on PI substrate with width/length of 50/10 µm. (b) Capacitance–voltage characteristics measured at 10 KHz. (c) MW tuning characteristics with hysteresis and (d) corresponding leakage current characteristics.

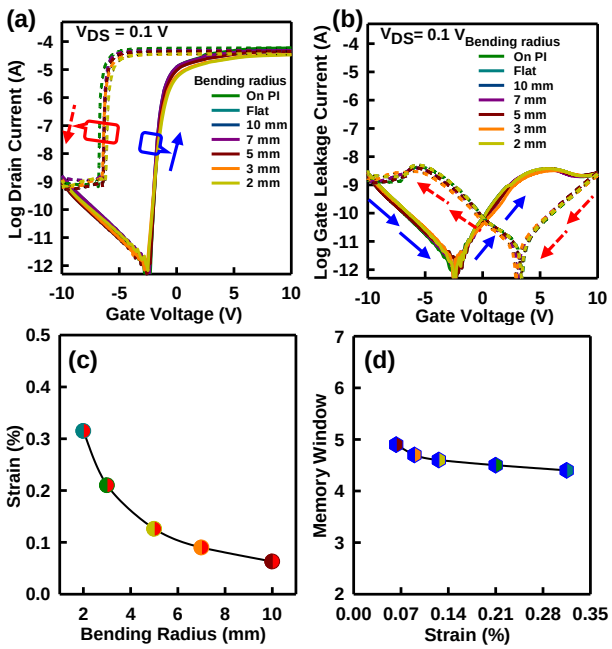

Figure 4. (a) Transfer characteristics and (b) Corresponding leakage current characteristics with different bending radius varied from flat to 2 mm. (c) Strain as a function of radius of bending. (d) Change of MW under different mechanical strains.

evaluated under various bending radii ranging from the flat to a 2 mm bent state. The corresponding I_{GS} vs V_{GS} curves exhibit no change in butterfly shape with current peaks at about V_{GS} of ±10 V regardless of the bending radius. The MBS applied to the FE-TFT due to bending with different radii was calculated using the formula:

$$\text{Strain} = (t_f + t_s)/2R \,, \quad \text{- - - - (1)}$$

where t_f is the thickness of the flexible substrate, t_s is the total thickness of the device, and R is the bending radius, as shown in Fig. 4(c). [1] Finally, Fig. 4(d) illustrates the change in MW as a function of strain up to 0.32%, revealing small MW variation of ~ 0.5 V shows nearly stable electrical properties even under high mechanical constraints. The strain induced during bending in FE-HZO is primarily concentrated at the interface between the HZO and the substrate. This strain can trap charges, pin domains, and hinder their switching, potentially leading to MW deterioration. **Table 1.** Represent the literature summary of the flexible ferroelectric HZO thin film transistors.

4. Conclusion

In summary, a high-performance flexible FE-TFT, using a thin (5 nm) c-IGZO channel and HZO ferroelectric material, was successfully made on PI substrate, addressing the challenges of ferroelectric memory on flexible substrate. Flexible HZO TFTs on a polyimide (PI) substrate via spray pyrolysis exhibit a large MW of 5 V at V_{GS} of ±10 V, a low subthreshold swing (SS) of 120 mV/decade, and high I_{ON}/I_{OFF} ratio of ~8.9×10^6. These flexible TFTs demonstrate robust electrical performance under MBS up to 0.32% with a radius of 2 mm. This indicates that flexible HZO FE-TFTs maintain high stability under against mechanical flexing and preserve ferroelectricity with negligible MW degradation, even at a 2 mm bending radius. Consequently, low-cost spray-pyrolyzed FE-HZO TFTs hold great promise for applications in nonvolatile memory and synaptic devices in future flexible electronics.

5. Acknowledgements

This work was supported by the National Research and Development Program through the National Research Foundation of Korea under Grant RS-2024-00406548.

Table 1. Literature summary of the flexible ferroelectric HZO thin film transistors

Substrate	Deposition process	Process Temperature	I_{ON}/I_{OFF} ratio	Polarization μC/cm^2	Memory Window (V)	Bending Type	Min. bending radius (mm)	Ref.
Mica	[c]ALD	[a]RTA 500 °C	6.5×10^5	30.8	0.6	Tensile	4	[11]
Mica	[d]PEALD	[b]FMA 250 ^{0}C	10^5	50	1.76	Tensile	2	[12]
Mica	ALD	RTA 400 ^{0}C	10^8	40	2.78	Tensile/ Compressive	7	[13]
PI	Spin Coating	450 ^{0}C	10^5	-	1.98	Tensile	2	[14]
PI	**Spray Coating**	**As deposited 350 ^{0}C**	**8.9×10^6**	**14**	**5 V**	**Tensile**	**2**	**Our work**

[a]RTA: Rapid thermal annealing, [b]FMA: Focused microwave annealing, [c]ALD: Atomic layer deposition, [d]PEALD: Plasma enhanced atomic layer deposition

6. References

1. Jiang J, Bitla Y, Huang C-W, Do TH, Liu H-J, Hsieh Y-H, et al. Flexible ferroelectric element based on van der Waals heteroepitaxy. Science Advances. 2017;3(6):e1700121.
2. Yu H, Chung C-C, Shewmon N, Ho S, Carpenter JH, Larrabee R, et al. Flexible Inorganic Ferroelectric Thin Films for Nonvolatile Memory Devices. Advanced Functional Materials. 2017;27(21):1700461.
3. Roy S, Islam MM, Ali A, Saha JK, Lee H, Tooshil A, et al. High Memory Window, Dual-Gate Amorphous InGaZnO Thin-Film Transistor with Ferroelectric Gate Insulator. physica status soli di (a).n/a(n/a):2400638.
4. Lee H, Islam MM, Bae J, Jeong M, Roy S, Lim T, et al. A Coplanar Crystalline InGaO Thin Film Transistor with SiO2 Gate Insulator on ZrO2 Ferroelectric Layer: A New Ferroelectric TFT Structure. Advanced Materials Technologies.n/a(n/a):2401075.
5. Chen Y, Yang Y, Yuan P, Jiang P, Wang Y, Xu Y, et al. Flexible Hf0. 5Zr0. 5O2 ferroelectric thin films on polyimide with improved ferroelectricity and high flexibility. Nano
6. Ali A, Islam MM, Billah MM, Roy S, Kim B, Rabbi MH, et al. High-quality a-InGaZnO and a-ZrAlO deposited at 375 °C by spray pyrolysis for low voltage operation TFTs. Materials Letters. 2024;367:136600.
7. Saha JK, Billah MM, Bukke RN, Kim YG, Mude NN, Siddik AB, et al. Highly Stable, Nanocrystalline, ZnO Thin-Film Transistor by Spray Pyrolysis Using High-K Dielectric. IEEE Transactions on Electron Devices. 2020;67(3):1021-6.
8. Saha JK, Roy S, Jang J. High-Dielectric-Constant MgZrO3 by Spray Pyrolysis for Thin-Fim Transistors in Low-Power Electronics. ACS Applied Electronic Materials. 2025. Research. 2022;15(4):2913-8.
9. Hasan MM, Roy S, Mohit, Tokumitsu E, Chu H-Y, Kim SC, et al. High performance, amorphous InGaZnO thin-film transistors with ferroelectric ZrO2 gate insulator by one step annealing. Applied Surface Science. 2023; 611:155533.
10. Kim Y-H, Lee E, Um JG, Mativenga M, Jang J. Highly Robust Neutral Plane Oxide TFTs Withstanding 0.25 mm Bending Radius for Stretchable Electronics. Scientific Reports. 2016;6(1):25734.
11. Liu H, Lu T, Li Y, Ju Z, Zhao R, Li J, et al. Flexible Quasi-van der Waals Ferroelectric Hafnium-Based Oxide for Integrated High-Performance Nonvolatile Memory. Advanced Science. 2020;7(19):2001266.
12. Joh H, Jung M, Hwang J, Goh Y, Jung T, Jeon S. Flexible Ferroelectric Hafnia-Based Synaptic Transistor by Focused-Microwave Annealing. ACS Applied Materials & Interfaces. 2022;14(1):1326-33.
13. Li Q, Wang S, Li Z, Hu X, Liu Y, Yu J, et al. High-performance ferroelectric field-effect transistors with ultra-thin indium tin oxide channels for flexible and transparent electronics. Nature Communications. 2024;15(1):2686.
14. Islam MM, Hasan MM, Jang J. High-Performance Flexible $Hf0.5Zr0.5O_2$ Ferroelectric Thin-Film Transistors on PI Substrate By Solution Process. ECS Meeting Abstracts. 2022; MA2022-02(15):812.