CMOS-Type Scan Driver Circuit Based on LTPO TFTs

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Abstract

We proposed a CMOS-type scan driver circuit using LTPO TFTs. The core logic part is designed as CMOS logic gates using LTPO TFTs, while the output part is composed of LTPS TFTs only to optimize the design area. In addition, double-gate structural Oxide TFTs are used to prevent operation in depletion mode. We confirmed that the output signal is stable through the fabricated circuit.

Author Keywords

Complementary metal-oxide-silicon; low-temperature polycrystalline silicon and oxide; thin film transistor; scan driver circuit; active-matrix organic light-emitting diode

1. Introduction

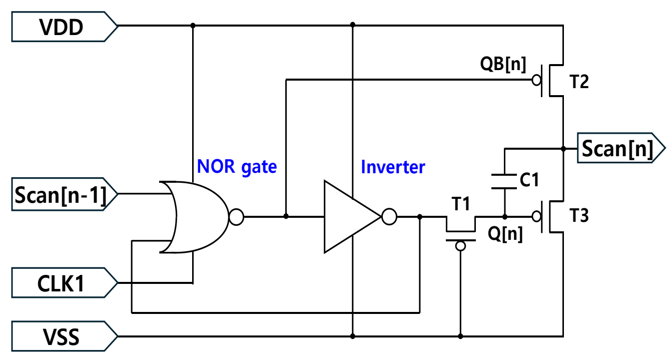
Active-matrix organic light-emitting diode (AMOLED) has been widely used in the display industry. Recently, AMOLED displays capable of both high and low refresh rates are required for mobile displays. To satisfy this requirement, pixel circuits have been designed by using the low-temperature polycrystalline and metal-oxide compound semiconductor (LTPO) technology. This structure generally consists of p-type low-temperature polycrystalline silicon (LTPS) thin film transistor (TFT) and n-type metal-oxide compound semiconductor (Oxide) TFT such as indium-gallium-zinc oxide (IGZO) TFT. In the pixel circuit using LTPO technology, LTPS TFTs are used for driving TFTs due to their excellent current driving capability, and Oxide TFTs are used as switching TFTs to maintain the gate voltage of the driving TFTs [1].

The scan driver circuit, which generates signals to control the switching TFTs in the pixel circuit, is integrated into the display panel to reduce the bezel size. Theoretically, the scan driver circuits can be implemented with complementary metal-oxide-silicon (CMOS) logic gates, using LTPO technology. However, the use of Oxide TFTs has been reported limitedly in the scan driver circuit, even with LTPO technology [2]. Because the mobility of Oxide TFTs is approximately 10% of that of LTPS TFTs. Therefore, the design area asymmetry between n-type and p-type TFTs is approximately ten times when applying conventional CMOS inverter structures to the output part using LTPO technology [3], [4]. In addition, n-type Oxide TFTs can exhibit a negative threshold voltage and operate in depletion mode, which leads to output voltage distortion and increased power consumption due to leakage current paths [5]. Therefore, depletion mode operation should be avoided when designing scan driver circuits with Oxide TFTs.

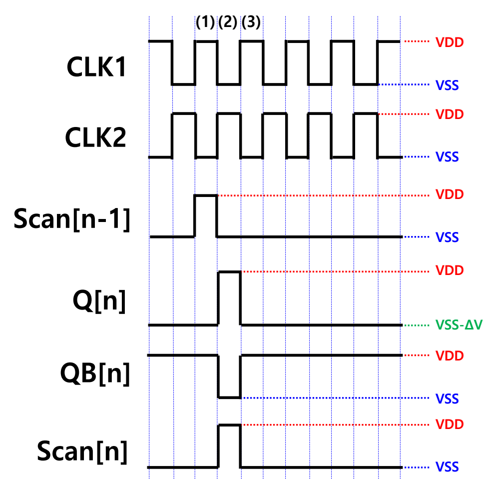
In this paper, we propose a CMOS logic gate-based scan driver circuit using LTPO technology. As mentioned above, there are two issues that need to be improved from the circuit design perspective when using Oxide TFTs in circuits. Therefore, the proposed scan driver circuit is designed with different concepts for the core logic and the output part, respectively. Also, an Oxide TFT with a double-gate structure is used to prevent depletion mode operation by applying a low-level DC voltage to the bottom gate electrode. In the output part, considering the effect of a large output load, only single p-type LTPS TFTs are used, excluding Oxide TFTs. Although p-type TFTs connected to high voltage can stably pull-up the output load, perfect pull-down operation cannot be achieved. To improve this, a bootstrapping method is employed to maintain a low gate voltage for the pull-down TFT, ensuring stable voltage output. Consequently, the proposed scan driver circuit is suitable for displays that require a narrow bezel and low power consumption.

2. Proposed Scan Driver Circuit

Figure 1 shows the logic and timing diagram of the proposed scan driver circuit consisting of nine TFTs and one capacitor. The CLK1 and CLK2 voltage are in the range of -8 to 8 V. Also, DC signals of VSS, VSSL, and VDD are -8 V, -10 V, and 8 V, respectively.

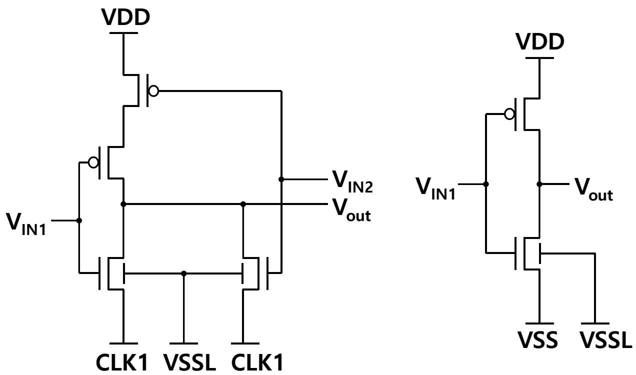


(a)



(b)

Figure 1. (a) logic diagram and (b) timing diagram of proposed scan driver circuit.



(a) (b)

Figure 2. (a) NOR gate structure and (b) inverter structure in the proposed scan driver circuit.

The proposed scan driver circuit applied NOR gate and inverter structure with p-type LTPS and n-type Oxide TFTs in the core logic part, as shown in Figure 1(a). The output part, which is affected by the large output load, consists of only three p-type LTPS TFTs and one capacitor. Figure 2 (a) and (b) show the NOR gate and inverter structure of the proposed scan driver circuit, respectively. We used the double-gate structural Oxide TFTs in the circuit. Therefore, Oxide TFTs in the scan driver circuit can stably operate under the enhancement mode by applying the lower negative voltage to the bottom gate electrode.

The operation of the proposed scan driver circuit can be divided into three periods. During the period (1), the high-level voltage of Scan[n-1] is applied to the input node of the NOR gate. This allows the high-level voltage of CLK1 to be applied to the gate node of the inverter. Subsequently, a low-level voltage is applied to the Q[n] node via the inverter. As a result, Scan[n] outputs VSS through T3. At the start of the period (2), Scan[n-1] temporarily maintains a high-level voltage due to the delay time. Meanwhile, the CLK1 signal changes to a low-level voltage of VSS, which is then applied to the gate node of the inverter and QB[n]. Consequently, T2 is turned on, causing Scan[n] to output VDD. Although the Scan[n-1] signal completely discharges to VSS, the QB[n] node remains at VSS since both the input voltages of the NOR gate are not low-level. In period (3), as CLK1 transitions to a high-level voltage, VDD is applied to the gate node of the inverter. This causes both inputs of the NOR gate to be at a low-level voltage. Additionally, bootstrapping occurs through C1 as a VSS is applied to the Q[n] node via the inverter. Therefore, Scan[n] stably outputs VSS by the low-level voltage bootstrapped to the Q[n] node.

3. Results and Discussion

We verified the operation of the proposed scan driver circuit using simulation (SmartSpice, Silvaco). The display panel has a resolution of 1440 × 2560 and a frame frequency of 120 Hz with one horizontal line time of 3.2 μs. We applied the scan-line load by a 10 kΩ resistor and a 22.5 pF capacitor to each output node. Figure 3 shows the measured and simulated transfer characteristics of LTPS TFT and the double-gate Oxide TFT used in the proposed circuit. The channel width/length of LTPS and the double-gate Oxide TFT was 5 μm/5 μm. The LTPS TFT shows a field-effect mobility (μ_{FE}) of 81.1 $cm^2/V{\cdot}s$ and a threshold voltage (V_{TH}) of -1.2 V. The double-gate Oxide TFT shows a μ_{FE} of 10.4 $cm^2/V{\cdot}s$ and a V_{TH} of -0.37 V at the bottom gate-to-source voltage (V_{BS}) is 0 V.

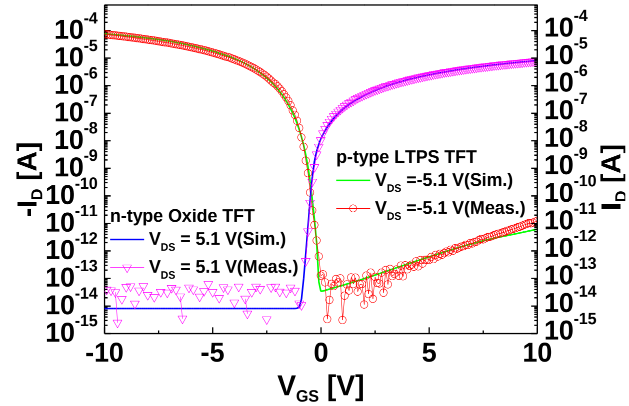


Figure 3. Simulated and measured transfer characteristics of p-type LTPS and n-type double-gate Oxide TFTs.

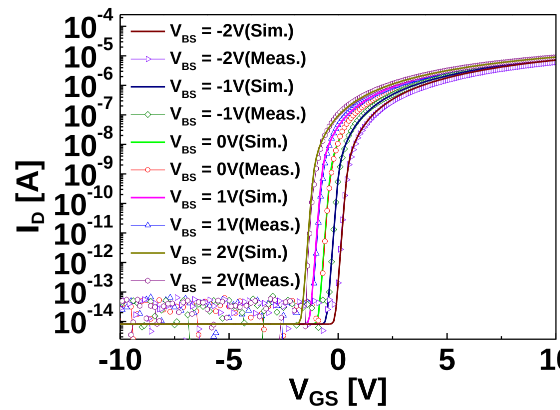


Figure 4. Simulated and measured transfer characteristics of the n-type double-gate Oxide TFT according to the bottom gate bias.

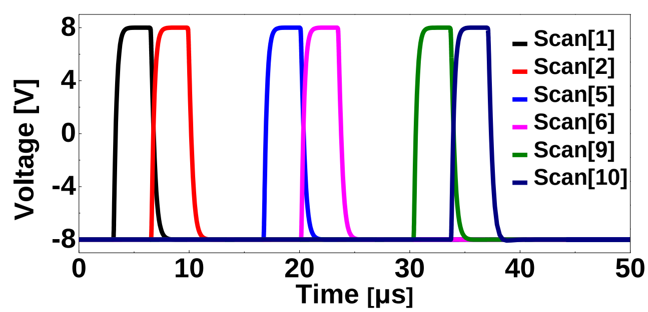


Figure 5. Simulated voltage waveforms of Scan[n] in multiple stages.

Figure 4 shows the measured and simulated transfer characteristics of the double-gate Oxide TFT according to the bottom gate bias, which is used in the proposed circuit. The simulated voltage waveforms of scan signals in multiple stages for the proposed scan driver circuit are shown in Figure 5. The nodes Q[n] and QB[n] are 8 V and -8 V, respectively, in period (2). Therefore, T3 is turned off and T2 is turned on, causing the scan signal to output 8 V. Subsequently, the node Q[n] is bootstrapped by C1 to reach approximately -15 V during the period (3). As a result, Scan[n] can stably output -8 V during the remaining frame time. Since the low-level voltage of VSSL is -10 V during circuit operation, the double-gate Oxide TFT can be stably turned off when its top gate-to-source voltage (V_{GS}) is 0 V.

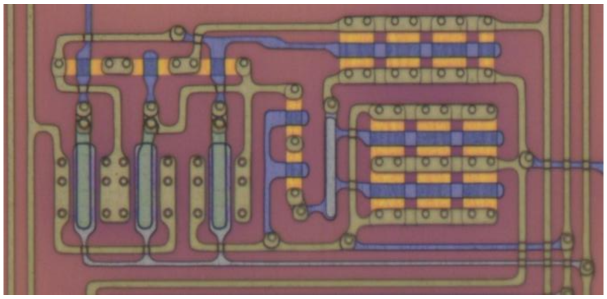


Figure 6. Microscope image of the proposed scan driver circuit.

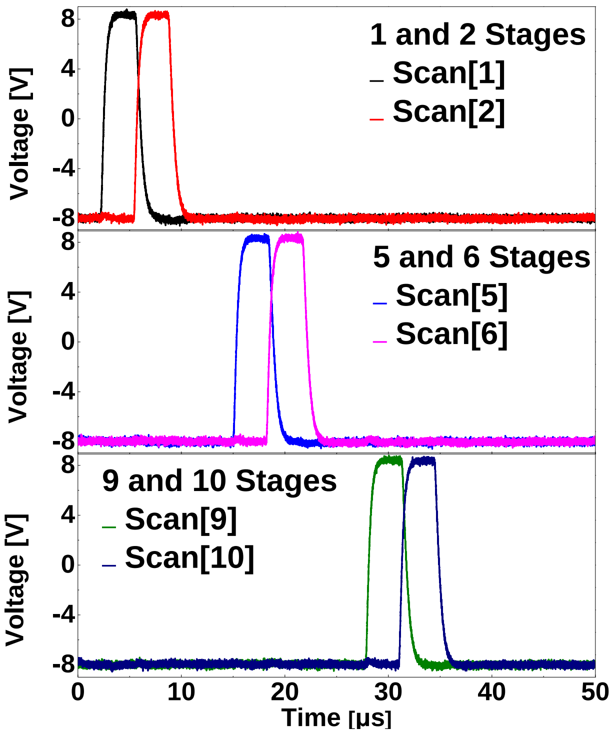


Figure 7. Measured voltage waveforms of the fabricated scan driver circuit in multiple stages.

We fabricated a scan driver circuit using double-gate Oxide TFTs and LTPS TFTs and verified the circuit operation. Figure 6 shows the microscope images of the proposed scan driver circuit. The measured voltage waveforms of the fabricated scan driver circuit with multiple stages are shown in Figure 7. The input signal of the fabricated scan driver circuit was applied using a pattern generator (EECHT01, ELP), and the output signals were measured using an oscilloscope (EXR058A, Keysight). Additionally, the measured signals were able to maintain a low-level voltage due to stable bootstrapping. Consequently, the fabricated scan driver circuit shows a shift register operation with stable output signals.

4. Conclusion

We proposed an LTPO TFT-based CMOS-type scan driver circuit. The core logic and output parts were designed with different concepts and structures. The core logic part is composed of CMOS logic gates using LTPO TFTs and successfully transmits two opposite signals to the output part. The output part was designed only with LTPS TFTs. The proposed circuit minimizes the design asymmetry of the output part by using LTPS TFTs, which have relatively higher mobility than that of Oxide TFTs. In addition, Oxide TFTs were used in a double-gate structure to prevent operation in depletion mode. The stable output signals of a scan driver circuit were verified through the output waveform of the fabricated circuit.

5. Acknowledgement

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6. Reference

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