Low-Power Gate Driver Circuit with Variable Pulse Width for LTPO-Based AMOLED Displays

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Abstract

Dynamic power consumption persists in the conventional gate driver circuit even during low-refresh-rate operation of OLED displays because oscillation of clock signals is required while outputting switch-off voltage level. To solve this problem, we propose a novel LTPO-based gate driver circuit that requires no clock signal oscillation under the low-refresh-rate condition, thereby effectively eliminating the dynamic power consumption.

Author Keywords

Low-Temperature Poly-Crystalline Silicon and Oxide (LTPO); active-matrix organic light-emitting diode (AMOLED); gate driver circuit; low power consumption.

1. Introduction

In recent years, mobile devices and various other display technologies have increasingly transitioned toward Organic Light-Emitting Diode (OLED) displays due to their superior image quality, free form factors and low power consumption. This shift has been supported by the development of LTPO backplane technology, which utilizes the low off-current characteristics of MOx. (Metal Oxide) TFTs to prevent the charge stored in the storage capacitors of the pixel circuit from leaking [1]-[2]. Therefore, it ensures that the display image remains stable during low-refresh-rate operation, while significantly reducing the power consumption of OLED displays. However, in mobile displays, gate driver circuits are predominantly based on p-channel LTPS TFTs due to their high current-driving capability and stable electrical characteristics, which enhance the circuit's reliability and operation. One critical function of the gate driver circuit is to output a low voltage level to turn off the n-channel MOx switch TFTs in the pixel circuit. These TFTs are turned off most of the time and are only activated during the reset and threshold voltage compensation phases of the pixel circuit. This requires the gate driver circuits to output a low voltage level over long periods of time. However, gate driver circuits using a p-channel LTPS pull-down buffer TFT to maintain a low voltage level for long durations have inherent problems. The high off-current of LTPS TFTs can cause the pull-down buffer TFT's gate voltage to rise, potentially turning off the buffer TFT, which poses a constraint on lowering the refresh rate. Although 1 Hz operation can be achieved by utilizing periodic bootstrapping or coupling effects through the CK signal to further lower the gate node voltage of the pull-down buffer TFT, gate driver circuits still suffer from significant dynamic power consumption even when operating at a low-refresh-rate due to the periodic charging and discharging of the capacitors connected to the clock signals [3].

In this paper, we propose an LTPO-based 7T-2C gate driver circuit that can operate at a refresh-rate of 1 Hz without the need for clock signal to oscillate, thereby eliminating dynamic power consumption during low-refresh-rate driving. The operation of the circuit, its verification using SPICE simulation, and the measurement results of the fabricated test samples will be presented.

2. Conventional LTPO based Gate Driver Circuit

Figure 1 (a) shows the schematic of the conventional 6T-2C LTPO-based gate driver circuit, which consists of five LTPS TFTs, one MOx TFT and two capacitors [4]. T5 and T6 pull-up and pull-down TFTs are both implemented using p-channel LTPS TFTs, therefore the gates of the buffer TFTs must operate in complementary states. To achieve this, the Q and QB node voltages are controlled through the inverter configuration by including n-channel MOx TFT T3. To output VGL voltage for long period of time with p-channel buffer TFT, Q node must maintain voltage lower than VGL. However, due to the high off-current of the T1 and T4 TFTs, Q node voltage gradually rises, which may cause the T6 pull-down TFT to turn off. Additionally, if the Q node voltage increases, it could cause the T3 MOx TFT, which operates in depletion mode, to turn on, potentially leading to leakage current and increased power consumption. Consequently, the high off-current of LTPS TFT imposes limitations on lowering the operation frequency.

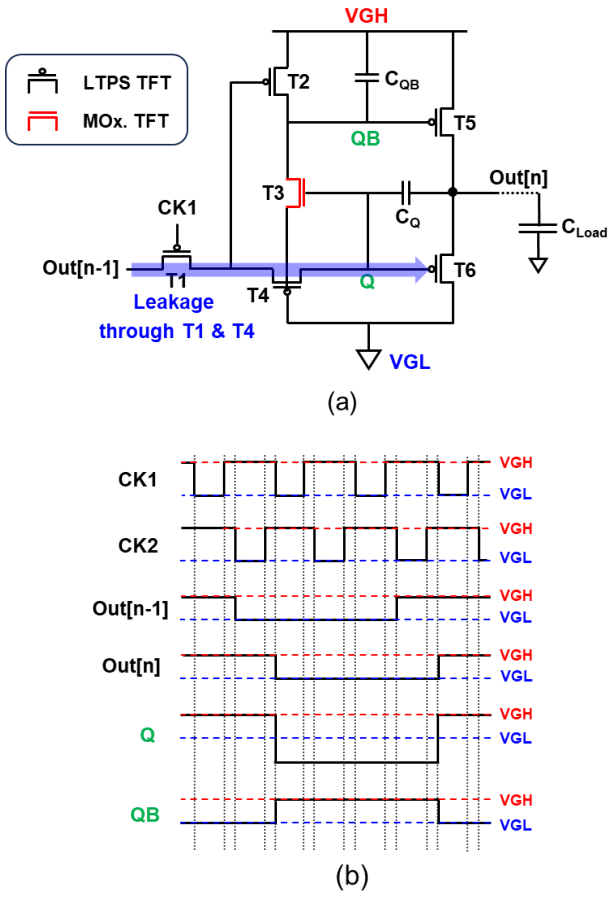

Figure 1. (a) Schematic and (b) timing diagram of conventional 6T-2C LTPO-based gate driver circuit

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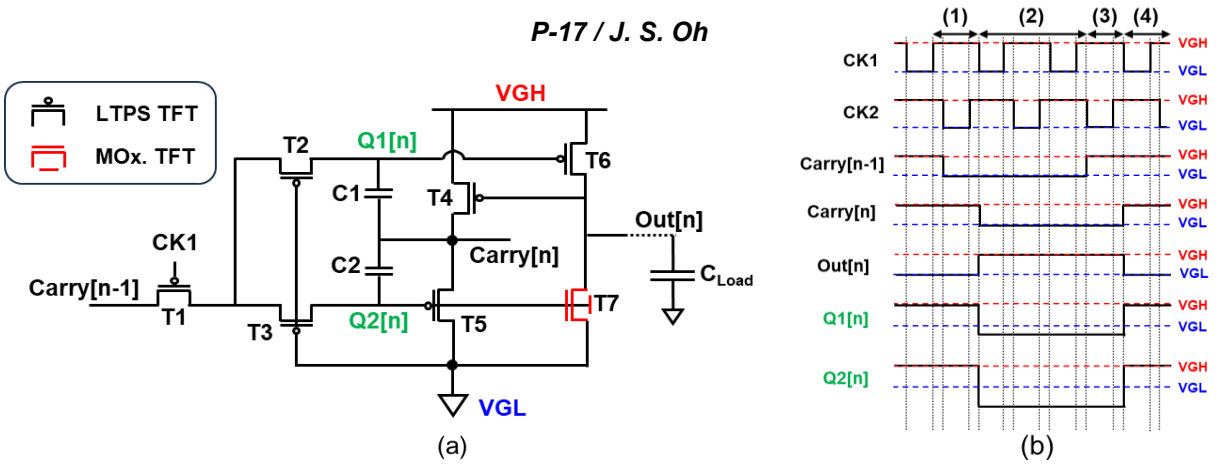


Figure 2. Proposed LTPO-based 7T-2C gate driver circuit (a) schematic and (b) timing diagram.

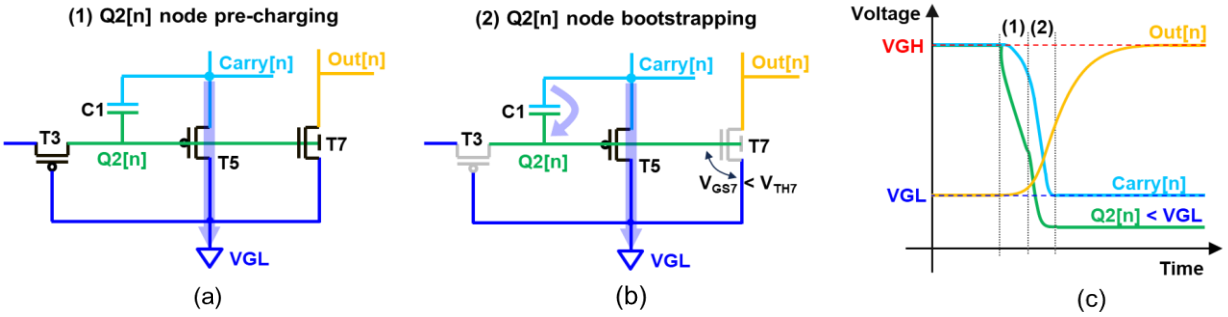


Figure 3. Operation of Q2[n] node bootstrapping: (a) Q2[n] node is discharged earlier than Carry[n] node, (b) Subsequent Carry[n] voltage pull-down causes bootstrapping at Q2[n] node. (c) Voltage waveforms of the Carry[n], Q2[n], and Out[n] during bootstrapping operation.

3. Proposed LTPO based 7T-2C Gate Driver Circuit

Figure 2 (a) and (b) show the schematic of the proposed LTPO-based 7T-2C gate driver circuit with its timing diagram. The proposed circuit is composed of six LTPS TFTs, one MOx TFT and two capacitors. The circuit utilizes two power signals, VGH and VGL and two clock signals. The output buffer of the proposed circuit is composed of CMOS inverter structure, formed by p-channel LTPS T6 and n-channel MOx T7 TFTs. Unlike conventional gate driver circuits, the Carry[n] and Out[n] signals are separated and have inverted voltage waveforms. When outputting the VGL voltage level, p-channel T4 TFT is turned on, maintaining Carry[n] voltage at VGH level. Since the Carry[n] signal is normally high and designed to pass only through p-channel TFTs, the VGH-level Carry[n] signal is delivered without any voltage drop. Therefore, all internal nodes of the circuit, except for the output node, are directly connected to VGH, which allows the voltage of the internal nodes to remain constant and prevents malfunction due to leakage current. As a result, the normally-high Carry[n] signal is applied to the CMOS inverter buffer structure, thereby turning on the NMOS pull-down buffer TFT, allowing the Out[n] signal to maintain a stable VGL voltage level for long periods of time.

To effectively utilize MOx TFTs in gate driver circuits, it is essential to turn them off completely due to their depletion-mode characteristics. High leakage current may lead to circuit malfunction or high-power consumption. The proposed circuit solves this issue by bootstrapping the Q2[n] node. When outputting the Carry[n] signal to the VGL voltage level, Q2[n] node voltage is lowered below VGL by the bootstrapping effect of the T5 and C2 capacitor. This ensures that T7 MOx TFT turns off with a negative V_{GS}, as illustrated in Fig. 3.

4. Operation Sequence of The Proposed Circuit

As illustrated in Fig. 2 (b), the operation of the proposed circuit can be divided into four stages. (1) VGL voltage holding period before pull-up, (2) Pull-up and VGH voltage maintenance, (3) VGH voltage holding period before pull-down, (4) Pull-down and VGL voltage maintenance.

(1) VGL voltage holding period before pull-up

Carry[n-1] signal transitions from VGH to VGL, but T1 TFT is turned off because the CK1 signal is held at VGH. As a result, the voltage change of the Carry[n-1] cannot be transferred to Q1[n] and Q2[n] nodes, allowing T7 TFT to be turned on and hold Out[n] to VGL voltage.

(2) Pull-up and VGH voltage maintenance

As the CK1 signal transitions to VGL, Q1[n] and Q2[n] nodes discharge, turning on the T6 pull-up TFT and charging Out[n] to VGH. Meanwhile, Q2[n] node is bootstrapped to a voltage lower than VGL by T5 TFT and C2 capacitor, ensuring that the MOx TFT T7 is fully turned off with a negative V_{GS} applied to its gate.

(3) VGH voltage holding period before pull-down

Carry[n-1] signal transitions from VGL to VGH, but since the CK1 signal remains at VGH, T1 TFT is turned off. As a result, the voltage change of the Carry[n-1] cannot be transmitted to the Q1[n] and Q2[n] nodes. This ensures that the Q1[n] and Q2[n] nodes maintain their voltage, allowing T6 TFT to remain on and hold Out[n] at VGH.

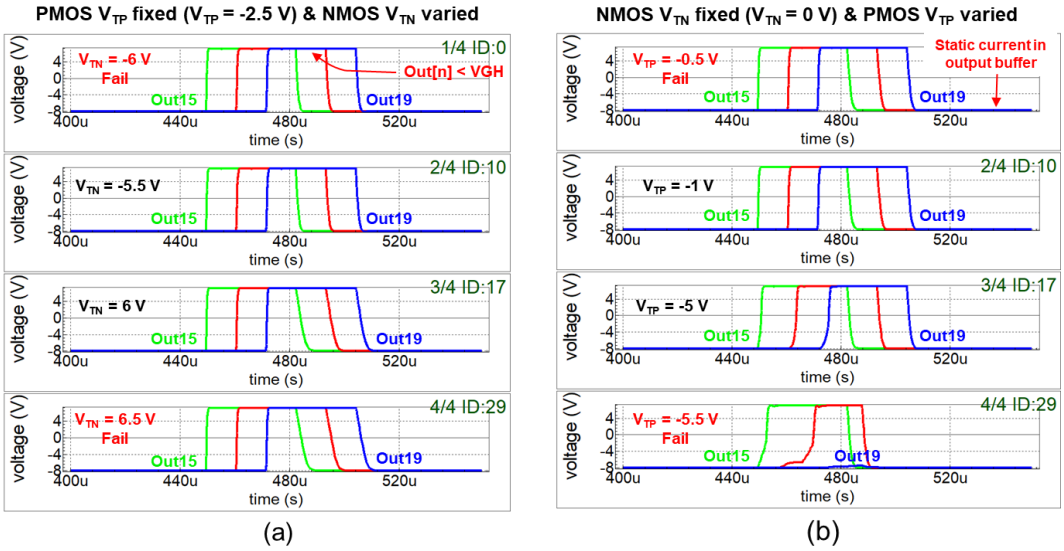


Figure 4. Output voltage waveforms of 15th, 17th, 19th stages with V_{TN} and V_{TP} varied at 120 Hz operation. (a) Output voltage waveforms for V_{TN} variation with V_{TP} = -2.5 V fixed. and (b) Output voltage waveforms for V_{TP} variation with V_{TN} = 0 V fixed.

(4) Pull-down and VGL voltage maintenance

As the CK1 signal transitions to VGL, T1 TFT turns on, charging Q1[n] and Q2[n] nodes to VGH. As a result, MOx T7 pull-down TFT turns on, discharging Out[n] to VGL. Consequently, T4 TFT turns on, charging the Carry[n] to VGH. Afterward, the CK signal toggles T1 TFT. However, since there is no voltage change in the Carry[n-1] signal, Q1[n] and Q2[n] nodes maintain VGH voltage, allowing the T7 MOx TFT to stably output VGL.

4. Results and Discussion

NMOS and PMOS V_{TH} operation margins, 1 Hz refresh-rate operation, and power consumption evaluation of the proposed 7T-2C gate driver circuit were verified using SmartSpice of Silvaco Inc. Thirty stages of the proposed 7T-2C gate driver circuit were cascaded and simulated with the parameters listed in Table 1.

Figure 4 shows the simulation results of the output voltage waveforms of the 15th, 17th, and 19th stages. To evaluate the operation margin of the NMOS threshold voltage (V_{TN}), PMOS threshold voltage (V_{TP}) was fixed to -2.5 V and V_{TN} was varied. Figure 4 (a) shows that the proposed circuit can operate within a V_{TN} range of -6 V < V_{TN} < 6.5 V. Conversely, to assess the operation margin of V_{TP}, the NMOS threshold voltage was set to 0 V and V_{TP} was varied. The simulation results show that the circuit can generate the output voltage waveforms of V_{TP} values ranging from -5 V < V_{TP} < -0.5 V, as illustrated in Figure 4 (b).

Figure 5 shows the output voltage waveforms of 1 Hz driving conditions. Validation of the proposed circuit's low-frequency operation was conducted with V_{TN} set to 0 V and V_{TP} set to -2.5 V. The simulation results show that the circuit successfully maintained VGH voltage level for 100 µs and VGL voltage level for 1 second during 1 Hz operation. Additionally, the clock signals were maintained at VGL voltage level to eliminate dynamic power consumption caused by the charging and discharging of the capacitors.

Power consumption was calculated under the assumption of a 3k display, operating at a 120 Hz refresh rate, with V_{TN} = 0 V and V_{TP} = -2.5 V. Although MOx TFTs operating in depletion mode may increase power consumption due to leakage current, bootstrapping the Q2[n] node to a voltage lower than VGL ensures that the MOx TFT is fully turned off by applying a negative V_{GS} to its gate. Furthermore, the elimination of charging and discharging of the internal capacitors contributes to reduced power consumption. As a result, the proposed circuit achieves power consumption as low as 1.42 mW.

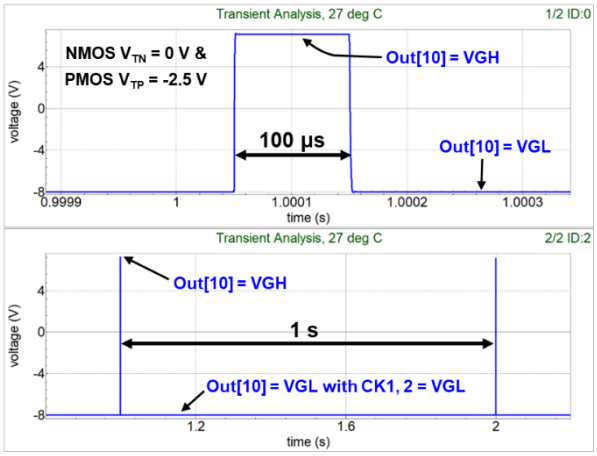


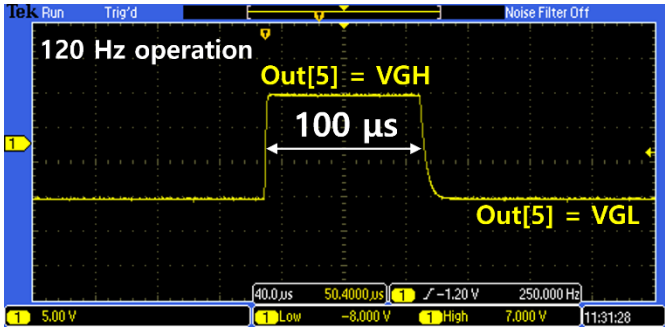
Figure 5. Output voltage waveforms of the 10th stage for 1 Hz operation with V_{TP} = -2.5 V, V_{TN} = 0 V.

Table 1. Design Parameters and values used in SPICE simulation

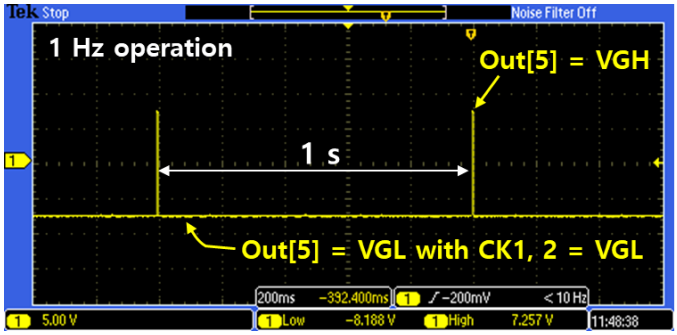
Parameters		Parameters	
VGH	7 V	W/L of T1, T2, T3, T4, T5	5 µm/5 µm
VGL	-8 V	W/L of T6	40 µm/5 µm
CK1, CK2	7 V/ -8 V	W/L of T7	40 µm/5 µm
C_{Load}	20 pF	C1	50 fF
R_{Load}	20 kΩ	C2	150 fF

5. Fabrication and Measurement Results

A test sample of the proposed 7T-2C gate driver circuit was fabricated. The output voltage waveform of the circuit was measured under refresh-rate of 120 Hz and 1 Hz operating condition. Figure 6 (a) shows the measured output voltage waveform of the 5th stage, which can output the VGH voltage for 100 μs—sufficiently long to turn on the switch TFTs in the pixel circuit and compensate for the threshold voltage of the driving TFT. Figure 6 (b) shows the output voltage waveform of the 5th stage under 1 Hz refresh-rate condition. Output voltage can maintain VGL voltage up to 1 second with the CK1 and CK2 signal voltages held at VGL level. This capability to hold the clock signal voltage, verified through measurement results, demonstrates the effectiveness of the circuit design in eliminating dynamic power consumption of the gate driver circuit during low-refresh-rate operation.



(a)



(b)

Figure 6. Measurement results of the fabricated 7T-2C gate driver circuit: (a) Voltage waveform of Out[5] for 120 Hz operation, (b) voltage waveform of Out[5] for 1 Hz operation with CK signal holding method.

6. Conclusion

In this paper, we propose a new LTPO-based 7T-2C gate driver circuit that can reduce the dynamic power consumption of OLED displays substantially. Proposed gate driver circuit maintains normally-low output voltage level to turn off the n-channel MOx TFT in the pixel circuit for a long time, e.g. one second and outputs high-voltage pulses periodically. By adopting n-channel MOx TFT as a pull-down output buffer and also by employing normally-high carry signal which is the inversion of the output signal, the static current in the output buffer can be blocked with a p-channel LTPS pull-up TFT. Accordingly, stable low-refresh-rate operation, i.e. 1 Hz is possible even though the MOx TFT has depletion mode characteristics. The proposed 7T-2C gate driver circuit requires no clock signal oscillation under the low-refresh-rate condition, thus effectively eliminating the dynamic power consumption. Simulation results show that the proposed circuit can work over a wide range of threshold voltages for both NMOS and PMOS transistors, under various refresh rate conditions from 1 Hz to 120 Hz. Measurement results further confirm that the fabricated circuit operates successfully at both 120 Hz and 1 Hz refresh rate even though the clock signal voltage holding method was used for the 1 Hz operation.

7. Acknowledgements

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8. References

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