Self-Aligned Bottom-Gate Top-Contact Vertical-Channel In-Ga-Zn-Oxide Thin-Film Transistor

Zicong Huang, Ioannis Kymissis**
***Dept. of Electrical Engineering, Columbia University, New York, NY 10027, USA**

Abstract

We show a simple process to produce a novel bottom-gate vertical-channel In-Ga-Zn-Oxide (IGZO) thin-film transistors (TFTs) with a 400-nm effective channel length. The process is made possible by the conformal deposition of IGZO. The reported device showed promising performance with at least 10^6 on-off current ratio and $112\ \mu A/mm$ current per channel width (both measured at $V_{ds} = 0.1\ V$), comparable to the state-of-the-art top-gate vertical-channel IGZO TFTs.

Author Keywords

Vertical Channel Transistor; In-Ga-Zn-Oxide; Thin-film Transistor;

1. Introduction

The Display industry is moving towards the next generation of technologies. While it is hard to predict whether it will be microLED, miniLED, next generation OLED, or other emerging technology, the requirement for backplane transistors that supply and control individual pixels will continue to be more demanding. More on-state current density, faster switching time, and low off-current (1) are certain to be required. Vertical-channel transistors (VCTs) are among the solutions for display backplanes. The VCTs can have extremely short channel lengths, enabling high current density and fast switch. Another advantage of VCTs is that they can be fabricated with a short channel length without requiring precise patterning techniques, providing better performance without significantly increasing the fabrication cost (2). For the display industry, In-Ga-Zn-Oxide (IGZO) transistors are popular in the research. IGZO is relatively easy to deposit, has a very low off-current, and offers high carrier mobility, making it one of the most promising semiconductor candidates for next-gen display technologies (3). The fact that we can deposit IGZO with RF sputter or ALD makes it possible to create a thin channel that covers a step edge. As a result, there have been a number of reports about IGZO vertical-channel transistors demonstrating impressive performance (4–8). One problem, though, is that most proposed structures can be classified as “top-gate,” where the gate dielectric and gate metal are deposited after the IGZO layer. There are unique benefits and challenges for top vs bottom-gate TFTs. For IGZO TFTs specifically, developing a bottom-gate device with the semiconductor deposited later in the process allows wider choices for the gate dielectric deposition techniques. It also offers potentially better reliability with positive bias-temperature stress (9). A bottom-gate VCT also brings the possibility of fabricating dual-gate VCTs, providing even better channel control for our short-channel VCTs.

Studies show that top-contact devices tend to have better electrical performance than bottom-contact devices (10). Most IGZO VCTs reported so far are bottom-contact, and it is hard to make top-contact transistors with existing vertical structures. This problem is also addressed in our proposed structure, which makes both the top-contact and bottom-contact transistors possible. Annealing is another vital part of the IGZO device. It is well-known that proper annealing is essential for good performance (11,12). A limitation of the top-gate device is that some uncontrolled annealing will happen during the gate dielectric and gate metal deposition. Bottom-gate transistors, however, deposit the active layer towards the end of the process, avoiding any uncontrolled annealing processes and providing a potentially more precise thermal budget for the devices.

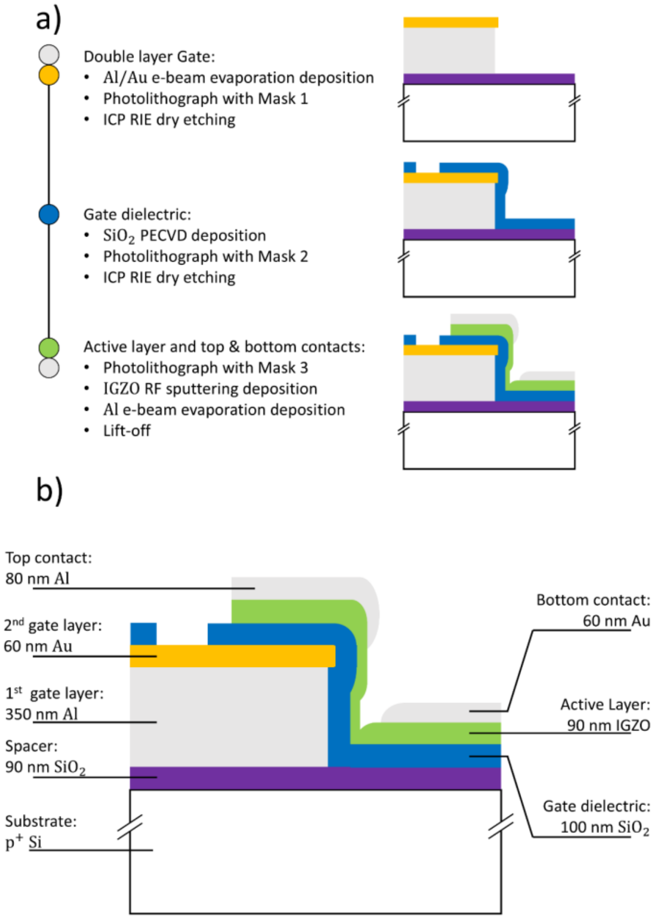

Figure 1. Bottom-gate IGZO step-edge vertical TFTs (BG-SEVTs) with about 450 nm channel length fabricated on a silicon wafer with thermal oxide (area **2x2 cm^2**): **a)** process flow and **b)** schematic cross-section.

Here, we report the bottom-gate top-contact VCTs we fabricated with precise sidewall profile control and self-aligned deposition of drain and source deposition.

2. Methodology

We fabricated bottom-gate top-contact step-edge vertical transistors (BG-SEVTs) with around 450 nm channel length on a silicon wafer with thermal-grown oxide (area 2x2 cm^2). The material and structure chosen are for fast prototyping. The fabrication steps and the cross-section of the finished transistor are schematically illustrated in **Fig. 1 a)** and **b).** We first deposited 350 nm-thick Al as the first layer of the gate electrode, followed

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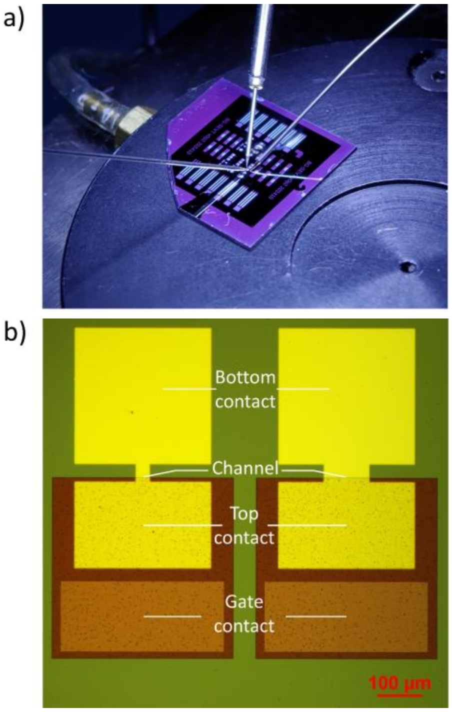

Figure 2. displays **a)** a photo of the measurement setup with probes on the sample; **b)** a micro-scope photo showing two transistors with 30 um (left), and 100 um (right) channel width. The corresponding parts of the transistors are annotated.

by 50 nm-thick Au within the same e-beam evaporation system without breaking the vacuum. We then pattern the gate electrodes with photolithography (mask 1). After that, we used ICP RIE to dry etch and remove the unprotected part. We first etch the Au layer with Ar milling with the native Al2O3 as the etch stopper. We then etch the Al layer with Cl-based chemistry and control the etching time carefully to avoid etching into the thermal SiO2. Next, we deposited 100 nm of SiO2 as the gate dielectric layer by PECVD at 300 ℃, followed by patterning by photolithography (mask 2) and F-based dry etching of the SiO2 layer with the Au layer as etch stopper. Finally, the lift-off structure for the channel and the top and bottom electrodes is prepared with photolithography (mask 3). The IGZO channel is then deposited using RF sputtering from a ceramic IGZO target. Due to the non-ideal conformality of the RF sputtering, the vertical channel is later measured to be 40 nm, which is thinner than the 90 nm lateral part. The 80 nm Al electrodes are thermally evaporated before we finish the lift-off as the last step.

Apart from using the layer thickness to define the channel length as many other vertical-channel IGZO transistors (4–8), the key innovation of the proposed structure is utilizing the difference in conformality of different deposition methods, namely the poor conformality of thermal evaporation and the relatively good conformality of RF sputtering, to create the top and bottom electrodes in one deposition step while also creating the channel that covers the side wall. The two-layer gate electrode, the choice of the etching gas, and the etching parameters are designed to achieve the ideal sidewall profile. Creating a little overhang of the Au layer is essential in our process. Such a sidewall profile of the gate electrode is crucial for three reasons. Firstly, we want to make sure that the top and bottom electrodes are separated from each other reliably. An undercut is needed for this reason. We also want to avoid a channel with breaking points since the step coverage ability of RF sputtering is not ideal. Last but not least, as Sun et al. pointed out in their study of a similar device structure but with ZnO as an active layer (13,14), too much undercut can result in prolonged un-gated channels near the bottom electrode, affecting the performance of the transistor. For these two concerns, too much undercut can be problematic. With our two-layer design, the top and bottom electrodes can be reliably isolated from each other, the channel is continuous, and there is minimal un-gated channel region.

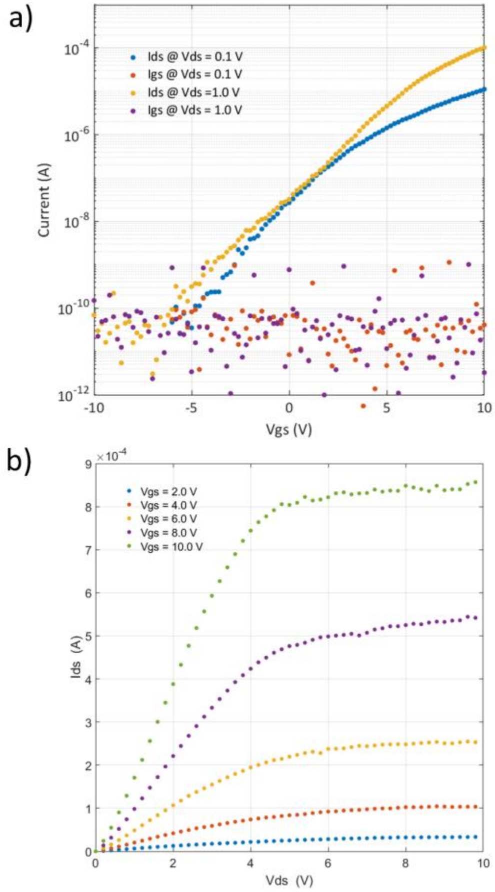

Figure 3. Electrical measurement results of the fabricated IGZO BG-SEVTs with $\mathbf{100\ \mu m}$ channel width: **a)** the transfer curves and the gate leakage current at $\mathbf{V_d = 0.1\ V}$ and $\mathbf{V_d = 1.0\ V}$. **b)** the output curves of the same transistor.

The optical photos of the completed sample are shown in **Fig. 2**

3. Results

Electrical measurements were made at room temperature in the air on a probe station in the dark. In our measurements, the bottom electrode is used as the drain electrode. In **Fig. 3a)**, the transfer curves in the linear regime with a drain voltage $(\mathbf{V_d})$ of 0.1 V and 1.0 V are shown for a BG-SEVT with $\mathbf{W/L}$ roughly as $\mathbf{100\ \mu m/0.4\ \mu m}$. The gate current is also shown in the same graph. It is not surprising that for such a short channel device, the on-current per width at $\mathbf{V_d = 0.1\ V}$ is relatively high at $\mathbf{112\ \mu A/mm}$. The linear and saturation mobilities are calculated as $\mathbf{0.3\ cm^2/V \cdot s}$. This low mobility is most likely because the

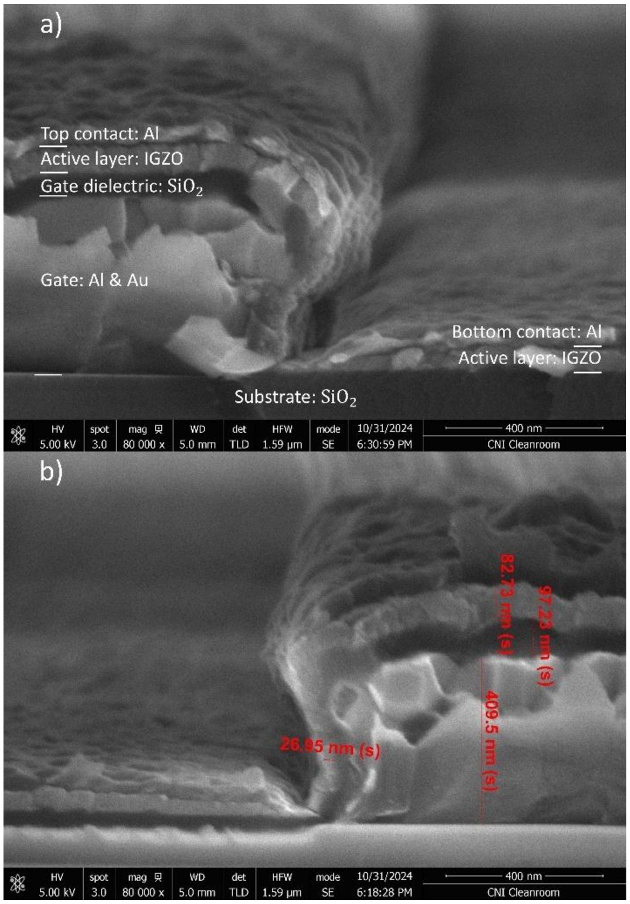

Figure 4. Cross-section SEM images of the fabricated BG-SEVTs: **a)** An image with the step on the left and the composition of the layers are annotated; **b)** An image with the step on the right, and the thickness of the layers are annotated.

sample hasn't been annealed when measured. The on-off ratio larger than $\mathbf{10^6}$ at $\mathbf{V_d = 0.1\ V}$ is comparable to some of the best top-gate SEVTs (6-8). We believe that the actual off current and the gate leakage are even lower, but the instruments used in our measuring set-up have a higher noise floor. The subthreshold swing of the device is 1.92 V/dec, which can be explained by the relatively thick **SiO2** dielectric layer.

The output curves for the same $100\ \mu\text{m}$ channel width BG-SEVT are shown in **Fig. 3b)**. The curves show good linearity near the left-side, indicating good ohmic contact, which is one of the motivations of making top-contact vertical channel IGZO transistors. The output curves also show good saturation among all the gate voltages tested. The curves become less smooth at high gate and drain-source voltage. It is possible that the self-heating of the device due to the large current density is playing a role there. The electrical measurements of the 18 BG-SEVTs over the 2x2 cm^2 sample show that the yield is 72% (13 out of 18). The current per width of the 10 µm-channel and 30 µm-channel transistors are roughly the same as the $100\ \mu\text{m}$ -channel transistors with variations within 30%.

After the electrical measurements, the sample was cleaved and examined with SEM. Two cross-section SEM images are shown in **Fig.4**. The two images display two edges facing opposite directions. The layers are easily recognizable in both images, indicating that we have successfully fabricated what we intended to. The SEM images confirm the intended small overhang of the second gate layer. It is also clear that the top and bottom electrodes are well separated, indicating that we can further shrink the channel length in the future. It is also evident that the IGZO layer on the sidewall is significantly thinner than the other lateral parts. This is not surprising since RF sputtering is known to have limited sidewall coverage ability. There are reports of IGZO deposited by plasma-enhanced atomic layer deposition (PEALD), which can offer better control of the thickness of the IGZO layer (15).

4. Future work

Molybdenum is widely used to create stable and lowest resistance contact for IGZO transistors. We plan to replace the Al top and bottom contact using Mo. The thickness of the gate dielectric is unnecessarily thick for the device to increase yield. If we replace the $100\ \text{nm}\ 300\ ℃$ PECVD SiO_2 with ALD HfO_2 or Al_2O_3, we can both drastically reduce the SS and also reduce the maximum temperature of the whole process to 150 C, opening more potential substrate choices. The gate layer thickness is also chosen for yield; based on the performance and the SEM images, we are confident that much shorter channel lengths are possible with a smaller gate layer thickness. To battle the possible short-channel effects, we plan to investigate the possibility of source-gated transistors (SGTs) by changing the contact material (16). The possibility of precisely controlling the IGZO annealing process is a key advantage for our bottom-gate device.

5. Conclusion

A novel bottom-gate top-contact step-edge IGZO thin-film transistor structure is proposed and successfully fabricated utilizing the conformality difference between deposition methods and the step-edge to self-align the top and bottom contacts. The transistors showed at least 10^6 on-off current ratio and $112\ \mu\text{A}/\text{mm}$ current per channel width (both measured at $\text{V}_{\text{ds}} = 0.1\ \text{V}$), good saturation in output characteristics, and ohmic contact behavior. The fabricated sample is also examined with cross-section SEM to verify that the intended structure is fabricated. We are also aware that the fabrication process still needs to be fully stabilized, many more characterizations need to be done, many obvious improvements should be made, and potential experiments can be done.

6. Acknowledgements

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