High Subthreshold Swing Using High-Performance Dual-Gate IZO/IGZTO TFTs for AMOLED Display

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Abstract

AMOLED displays at low gray levels require high SS to control the data potential easily. In this study, we present a high-mobility, coplanar dual-gate (DG) dual-channel TFT, where the SS can be tailored. This approach enables the device to function effectively as a driving TFT, achieving SS of 0.618 V/dec. The proposed DG, dual-sweep (DS) a-IZO/a-IGZTO TFT exhibits μ_{FE} of 65 cm²/V.s, V_{TH} of 0.46 V, and on/off current ratio of 10^8.

Keywords

a- IZO/a-IGZTO; dual active layer; coplanar dual gate TFT; modulated SS; gate potential effect

1. Introduction

Switching TFTs in AMOLED pixel and scan drivers require high μ_{FE}, low subthreshold swing (SS), and minimal off-state currents to achieve low driving voltage and low power consumption. Meanwhile, pixel-driving transistors connected to OLED diodes demand a high SS (≥ 0.5 V/decade) at low gray levels [1-3] [5-8]. Therefore, extensive research is focused on tailoring SS, where DG dual channel TFTs offer promising approach to achieve optimized SS and enhanced stability. However, high-field effect mobility (μ_{FE}) TFTs tend to exhibit small SS, which may not be ideal for driving TFTs. The OLEDs can function effectively under subthreshold conditions and drive low gray levels requiring high SS [5-15]. When dealing with low gray levels, the display needs precise control over voltage and current to reproduce the color correctly to maintain high contrast ratio [9]. High SS ensures that low intensity light can be accurately reproduced without unnecessary energy consumption. High SS also maintain smooth transitions between dark shades without color shifting, which helps to have better image quality [11]. Without high SS for low gray level, we may see more light leakage which will reduce display's overall contrast and image quality. In DG TFTs, the bottom gate (BG) can provide a higher SS, suitable for driving TFTs operating in subthreshold conditions. Note that bulk-accumulation in DG can have small SS for the TFTs for switching functionality.

In this work, we studied the DG dual channel, coplanar a-IZO/a-IGZTO TFT, exhibiting V_{TH} of 0.95 V for bottom sweep (BS), -0.35 V for top sweep (TS) and 0.46 V dual sweep (DS), and SS of 0.618 V/dec for BS, 0.220 V/dec for TS and 0.200 V/dec for DS, and μ_{FE} of 30.63 cm^2/V.s (BS), 54.99 cm^2/V.s (TS), and 65.81 cm^2/V.s for DS with all high on/off current ratio of 10^8.

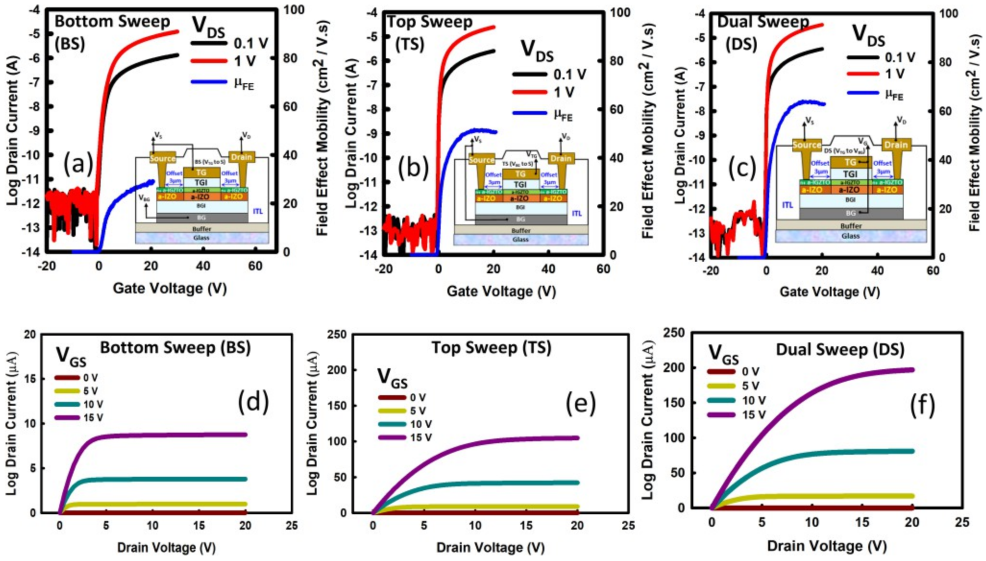

Figure 1: Transfer characteristics along with the inset represents TFT operation of (a) Bottom sweep (BS), (b) Top sweep (TS) and (c) Dual sweep (DS) at V_{DS} = 0.1 V and 1 V. Output characteristic of at V_{GS} = (0 V, 5 V, 10 V, 15 V (d) bottom sweep (BS), (e) top sweep (TS) and (f) dual sweep (DS)

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By applying the top-gate (TG) connection to the source, we achieved high SS, making it suitable for driving TFT for low gray levels. Note that low SS was observed in both TS and DS operations, making them ideal for switching TFTs. These results suggest that the a-IZO/a-IGZTO TFT, with its high mobility could be suitable for large area, high resolution AMOLED and AMLED displays.

2. Experimental Section

The fabrication process of DG dual channel, a-IZO/a-IGZTO TFTs with a self-aligned coplanar structure uses the following steps. First, a 350 nm thick SiO_2 buffer layer was deposited on glass. Then, a 100 nm thick Mo layer was deposited as a BG and then patterned. A 350 nm SiO_2 layer was deposited to serve as the BG insulator (BGI). Then, the dual channel of a-IZO (In:Zn:O = 5.3:1:9) and a-IGZTO (In:Ga:Zn:Sn = 4:1:4:1) were deposited by sputtering. A 150 nm thick SiO_2 layer was deposited as a TG insulator (TGI) and a 150 nm Mo was deposited as a TG. An interlayer of 400 nm SiO_2 was deposited and then patterned. The source and drain electrodes were formed using a 230 nm Mo layer.

All electrical performances were measured using an Agilent 4156C semiconductor parameter analyzer. The V_{TH} was defined as the gate voltage (V_{GS}) corresponding to a constant drain current (I_{DS}) of W/L x 10 pA at the drain voltage (V_{DS}) of 0.1 V, where W is the TFT channel width and L is the length. The SS was calculated as $(d\log(I_{DS})/dV_{GS})^{-1}$ over the range of 10 pA ≤ I_{DS} ≤ 10 nA, with V_{DS} = 0.1 V.

3. Results and Discussion

Fig. 1 shows the transfer and output characteristics of bottom sweep (BS), top sweep (TS), dual sweep (DS) operations of coplanar DG, dual channel TFT with channel width (W)/ length (L) of 8/8 µm. BS was measured with the TG connected to the source, TS means the BG being connected to the source and DS is both gates being electrically connected as illustrated in the inset with TFT structure. Fig. 1(a-c) shows the transfer characteristics of BS, TS and DS operations respectively at V_{DS} = 0.1 V and 1 V. The V_{TH} of 0.95 V for BS, -0.35 V for TS and 0.46 V for DS, and SS of 0.618 V/dec (BS), 0.220 V/dec (TS), and 0.200 V/dec (DS). The μ_{FE} of 30.63 cm^2/V.s for BS, 54.99 cm^2/V.s for TS, and 65.81 cm^2/V.s for DS. Fig. 1(d-f) shows the output characteristic of BS, TS and DS respectively at V_{GS} = 0 V, 5 V, 10 V, 15 V and V_{DS} from 0 V to 20 V**.**

Fig. 2 (a) shows the transfer characteristic of BS operation when V_{TG} potentials are -5, -10, 0, 5, 10 V respectively. The V_{TH} are 14.40, 10.60, 0.95, -18.40, -24.60 V respectively at V_{DS} = 0.1 V. Fig. 2(d) shows the SS of 0.630, 0.628, 0.618, 0.645, 0.650 V/dec when V_{TG} are -5, -10, 0, 5, and 10 V respectively. On the other hand, Fig. 2 (b) explains the transfer characteristic of TS operation. Fig. 2 (e) shows the SS less than 0.225 V/dec when V_{BG} potentials are varied. The transfer characteristic of DS operation can be seen in Fig. 2(c), where the V_{GS} sweeps ±30 V and the SS remains constant at 0.200 V/dec. The results indicate that the DS and TS operations are excellent as switching TFTs.

The positive bias temperature stress (PBTS) tests were conducted for BS, TS and DS operations respectively at V_{DS} = 1.0 V with stress voltage of 20 V for 1 h as shown in Fig.3. Fig.3 (a) shows the PBTS for BS, when the stress voltage was applied to the BG with TG being connected to the source. The shift in V_{TH} was 0.58 V. The PBTS at TS was conducted when the stress was applied to the TG with BG being connected to the source. The resulting ΔV_{TH} was 0.50 V as shown in Fig 3(b). This positive shift in both TS & BS is attributed to electron trapping. On the other hand, when the stress potential was applied to both TG & BG in DS operation, there is no shift in the V_{TH} (ΔV_{TH} = 0 V) as shown in Fig. 3 (c).

Table 1 explains the summary of the electrical characteristic of BS, TS and DS TFT performances at V_{DS} = 0.1 V. Table 2 summarizes the comparison with the reported studies on DG

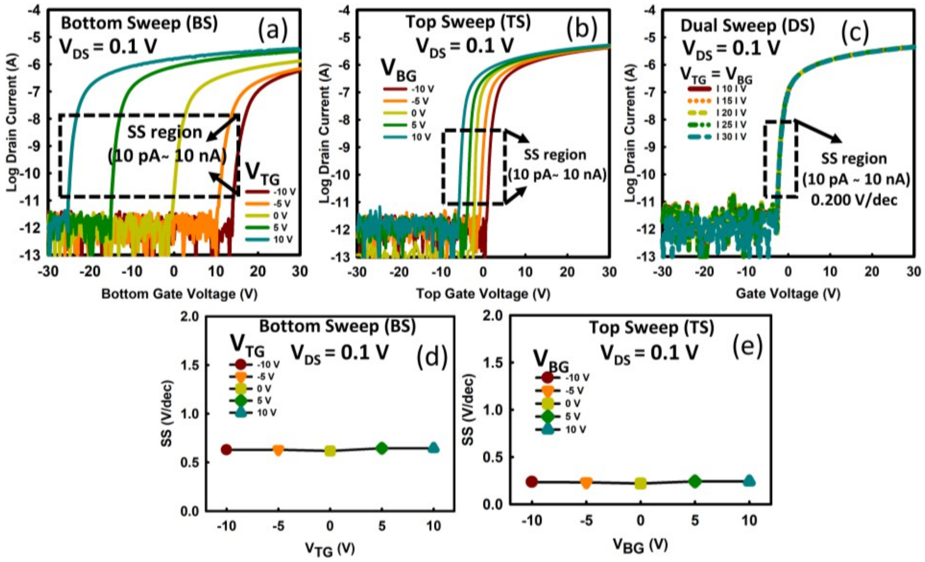

Figure 2. Transfer characteristics at V_{DS} = 0.1 V, (a) Bottom sweep (BS) operation when TG bias provided at (-5 V, -10 V, 0 V, +5 V, +10 V), (b) Top sweep (TS) operation when BG bias provided at (-5 V, -10 V, 0 V, +5 V, +10 V), (c) Dual sweep (DS) operation when both gates are connected and V_{GS} sweep for ±30 V. Subthreshold swing (SS) achieved at 10 pA ≤ I_{DS} ≤ 10 nA at V_{DS} = 0.1 V for (d) BS at TG bias, and (e) TS at BG bias

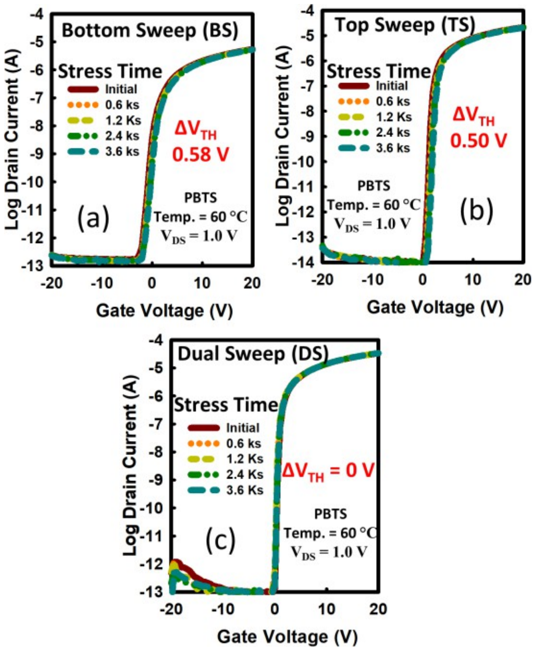

Figure 3. Transfer characteristics under positive bias temperature stress (PBTS) at 20 V: (a) BS, (b)TS, (c) DS at V_{DS} = 1.0 V for 1 h.

Table 1: Summary of electrical performances for driving TFT.

Sweep	μ_{FE} (cm^2/V.s)	V_{TH} (V)	SS (V/dec.)
BS	30.63	0.95	0.618
TS	54.99	-0.35	0.220
DS	65.81	0.46	0.200

Table 2: Summary of electrical performances reported in the literatures for oxide driving TFT of AMOLED displays

Structure	W/L (um)	μ_{FE} (cm^2/V.s)	SS_{max} (V/dec.)	V_{TH} (V)	Ref
DG	25/6	35.5	0.242	0.85	[1]
DG	3/3	21.01	0.21	-0.91	[2]
DG	3/3	-	0.350	-0.5	[3]
SG	40/20	4.9	0.590	-	[4]
SG	40/20	4.33	0.450	0.16	[5]

TFTs, highlighting the role of the back gate potential for achieving high SS for driving TFTs in AMOLED display at low gray levels. Note that when BS is used as the driving TFT, significantly higher SS of 0.618 V/dec could be achieved. The data reported in Ref [1-5] indicate the SS being less than 0.450 V/dec. In contrast, our device shows much higher SS of 0.618 V/dec so that can be useful to use as a driving TFT in AMOLED display for better low gray levels. Note that all the data on the PBTS for the dual gate TFTs show stable performance.

4. Conclusions

We report the application of dual gate IZO/IGZTO TFTs for AMOLED display. BS operation in dual gate structure increases the SS significantly. The TS or DS operation exhibits small SS compare to BS operation. This tailored SS can be helpful for driving AMOLED displays. The DG TFT, both TS and DS are excellent choice for switching TFT and BS for driving TFT. The proposed dual channel TFT provides high mobility with excellent stability. The dual channel, dual gate TFT provides μ_{FE} of 65.81 cm^2/V.s and ΔV_{TH} = 0 V at PBTS test, demonstrating the excellent TFT performance for TFT gate drivers and pixel circuits in AMOLED display.

5. Acknowledgements

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