Degradation Analysis of Organic Charge-Generation Layer by Impedance Spectroscopy

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Abstract

Understanding the degradation mechanisms of the charge generation layer (CGL) is critical for developing stable tandem organic light-emitting diodes (OLEDs). Capacitance-voltage measurements and modulus spectroscopy revealed that dopant diffusion at the CGL interface increases driving voltage. Equivalent circuit modeling confirmed resistance/capacitance shifts, guiding CGL optimization for enhanced stability.

Author Keywords

OLED; charge generation layer; impedance spectroscopy; modulus spectroscopy; degradation

1. Introduction

Tandem organic light-emitting diodes (OLEDs), featuring stacked emitting layers interconnected by a charge generation layer (CGL), offer enhanced brightness, efficiency, and operational lifetimes. The CGL, typically a p-n heterojunction, must balance high charge generation efficiency, rapid transport, low injection barriers, and optical transparency to optimize device performance.[1] However, long-term stability remains a critical challenge due to voltage instabilities linked to CGL degradation.[2,3]

Impedance spectroscopy has proven effective for probing carrier dynamics in OLEDs, particularly through dynamic modulus plots (DMPs) that visualize charge density variations across multi-layered structures.[4,5,6] This method, validated in our prior studies on double-layered electron blocking layers (EBL), provides a powerful tool to resolve interfacial charge behavior in complex device architectures.[7]

In this study, we employ DMPs to analyze degradation in CGLs within fabricated charge generation units (CGUs). By integrating capacitance-voltage measurements, DMP visualization, and equivalent circuit modeling, we identify dopant diffusion as the primary driver of CGL electrical degradation. This approach quantifies critical parameters governing CGL stability, offering insights for designing robust tandem OLEDs.

2. Experimental Details

2.1. Device Structures

The charge generation unit (CGU) structures investigated in this study consist of the following multilayer stack: Anode | NCGL | PCGL | HTL | HIL | Cathode. Here, NCGL refers to the n-doped charge generation layer, while PCGL and HIL denote the p-doped charge generation layer and the hole injection layer, respectively. The HTL (hole transporting layer) facilitates hole transport within the device. All OLED devices were fabricated using a vacuum evaporation process and encapsulated immediately after evaporation. This study involved the fabrication of two distinct device configurations:

Device A: Anode | Yb-doped NCGL (20 nm, 0.5 vol%) | p-doped PCGL (10 nm, 7.0 vol%) | HTL | HIL | Cathode

Device B: Anode | Yb-doped NCGL (20 nm, 2.0 vol%) | p-doped PCGL (10 nm, 7.0 vol%) | HTL | HIL | Cathode

2.2. Measurements and Characterization

Impedance spectroscopy was performed using a Solartron 1260A impedance/gain-phase analyzer. The frequency range was set from 0.1 Hz to 100 kHz, with an AC amplitude of 100 mV. The resulting capacitance and resistance values were extracted through equivalent circuit simulations using the Zview program, which enabled detailed analysis of the device's electrical properties. For capacitance-voltage (C-V) measurements, the DC voltage was varied from 0 V to 3 V in increments of 0.05 V, with an AC amplitude of 100 mV at a fixed frequency of 1000 Hz.

As demonstrated by J.-i Takahashi and H. Naito, modulus spectroscopy is a powerful tool for visualizing the complex voltage-dependent behavior and carrier distribution in OLED devices.[5,6] The complex impedance (Z) of a parallel RC circuit is described by the following equation:

$$Z = \frac{R}{1 + j\omega RC}, \tag{1}$$

where j is the imaginary unit, ω is the angular frequency, and R and C represent the resistance and capacitance, respectively. The modulus (M) is defined as:

$$M = j\omega Z = \frac{1}{C}\left(1 - \frac{1}{1 + j\omega RC}\right). \tag{2}$$

The plot of the real and imaginary parts of M is referred to as the Cole-Cole or Nyquist plot, while the plot of frequency versus the imaginary part of M is known as the Bode plot. A multi-layered OLED structure can be modeled as a series of RC circuits, with each organic layer represented as a parallel RC circuit, forming several semicircles in the Cole-Cole plot. In impedance and modulus Cole-Cole plots, the semicircle diameters correspond to R and $1/C$, respectively. The thickness (d) of the capacitor is given by $d=\varepsilon S/C$, where ε is the dielectric constant of the layers, and S (2*2 mm^2) represents the active area. Thus, the diameter of the semicircle in the modulus Cole-Cole plot is proportional to the thickness of the organic layer. The real part in the modulus Cole-Cole plots can be converted into the film thickness of organic layers, enabling the visualization of conductivity differences across each layer.[5,6,7]

3. Results and Discussions

3.1. Capacitance

As illustrated in Figure 1 (a), the PCGL and NCGL are fabricated with a high doping ratio, leading to significant band bending and the formation of a depletion region at the p-n heterojunction due to the high carrier concentration. Electrons are generated at the lowest unoccupied molecular orbital (LUMO) of the PCGL dopant, while holes are formed at the highest occupied molecular orbital (HOMO) of the PCGL host. Electron tunneling occurs from the LUMO of the PCGL dopant to the LUMO of the NCGL host.[1,3]

We observed the voltage trends for NCGL at various Yb-doping concentrations and selected 0.5 vol% (non-saturated concentration) and 2.0 vol% (saturated concentration) as

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representative cases to fabricate the corresponding CGU devices. The current-density-voltage (J-V) curves of Devices A and B are presented in Figure 1 (b). Based on the J-V curves, CGU devices with a Yb doping concentration of 2.0 vol% (Device B) exhibit higher conductivity due to their increased carrier density. However, no significant difference is observed in the onset voltage.

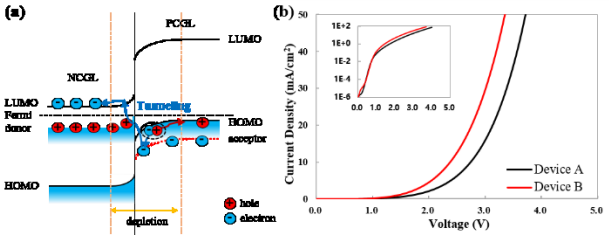

Figure 1. (a) Energy band diagram of the CGU devices. (b) J-V curves of Devices A and B, with the inset showing the exponential J-V plot.

A constant current density of 50 mA/cm² was applied to Devices A and B for 63 hours, under thermal stress at 85 °C (358 K). The voltage shift is shown in Figure 2 (a), indicating that Device B exhibits a larger driving voltage shift.

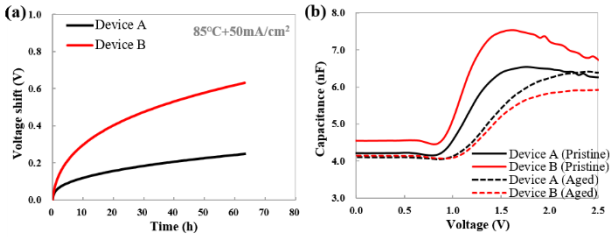

Figure 2. (a) Driving voltages of Devices A and B. (b) C-V curves for pristine and aged CGU devices.

The capacitance-voltage (C-V) curves of both pristine and aged CGU devices are shown in Figure 2 (b). The capacitance behavior can be divided into four distinct phases as the bias voltage increases: (1) At low voltages, no charges are generated in the CGL or injected from the electrodes, resulting in a constant geometrical capacitance. In aged devices, the reduction in geometrical capacitance is likely due to the diffusion of Yb atoms from the NCGL into the adjacent PCGL, leading to impurity compensation and a weakening of the p-doping effect. This effect is more pronounced at higher Yb-doping concentrations (e.g., NCGL = 2.0 vol%). Therefore, the aged Device B exhibited the smallest capacitance after the device turned on as shown in Figure 2 (b).[1,3] (2) At around 0.6 V, charge separation at the p-n junction widens the depletion region, causing a slight capacitance decrease. (3) At higher voltages (0.8 V ~ 1.5 V), the capacitance increases due to the enhancement of drift capacitance in the CGU devices, driven by the injection of majority charges generated at the p-n junction.[8] (4) Above 1.5 V, capacitance gradually decreases as carriers generated in the CGL flow out through the electrodes. In aged devices, reduced carrier generation in the CGL lowers the maximum capacitance and shifts the peak capacitance to higher voltages.

3.2. Modulus Spectroscopy

To more clearly identify the organic layer responsible for the charge changes observed in the C-V curves, we utilized modulus spectroscopy. Figure 3 illustrates a comparative analysis of the modulus Cole-Cole and Bode plots for Devices A and B, both before and after aging. Through modulus spectroscopy, we investigated the carrier distribution within the CGU devices under varying voltages. By adjusting the thickness of each layer, we identified and marked the corresponding regions of each functional layer in the modulus Cole-Cole plots. And the Bode plots exhibit distinct peaks corresponding to each Debye relaxation element, with the relaxation time (τ) derived from the inverse of the peak frequency.[5,6] The peak frequencies (f_{peak}) are related to the differential conductivities (σ) by the following equation:

$$f_{peak} = \frac{1}{2\pi\tau} = \frac{\sigma}{2\pi\varepsilon}. \quad (3)$$

According to Equation 3, the intrinsic layer, such as the HTL, generally exhibits lower conductivity compared to the doped layer. Consequently, the corresponding peak frequency is observed in the low-frequency range. From the Bode plot (Figure 3 (b)), in the pristine Device A, the depletion layer is observed near 200 Hz, while the n-doped layer appears around 5000 Hz. The p-doped layer, which possesses significantly higher conductivity than the other layers, is not detected within the tested frequency range.

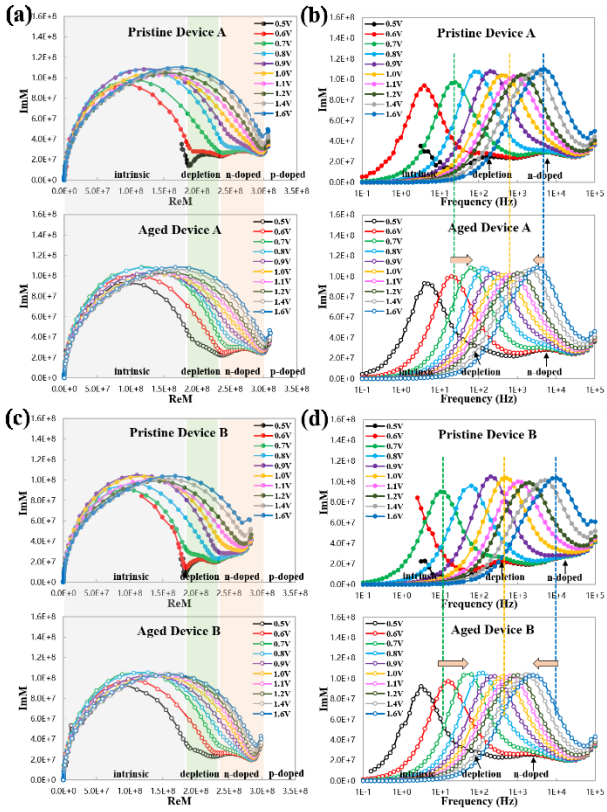

Figure 3. (a) The Cole-Cole plots and (b) the Bode plots of the pristine and aged devices under different DC bias voltages for Device A (NCGL = 0.5 vol%), and (c), (d) for Device B (NCGL = 2.0 vol%).

In the modulus Cole-Cole plots of the pristine devices (Figure 3 (a) and (c)), the valley depth between the intrinsic, depletion, and doped layers in Device B is deeper than that in Device A at the same voltage. Correspondingly, the Bode plots (Figure 3 (b) and (d)) exhibit higher peak frequencies for the depletion and n-doped layers in Device B. These phenomena can be attributed to the higher Yb-doping concentration in Device B. The increased doping reduces the depletion layer width, which enhances the tunneling probability of charge carriers. Consequently, this leads to an improvement in the conductivity of both the depletion and n-doped layers. The increased conductivity reduces the relaxation time of these layers, resulting in a more pronounced relaxation time difference between the intrinsic layer and the depletion/n-doped layers. This difference is reflected in the deeper valleys in the Cole-Cole plots. Simultaneously, the higher conductivity of the depletion and n-doped layers shifts their relaxation peaks to higher frequencies in the Bode plots.

As the voltage increases, the semicircles in the Cole-Cole plots gradually merge into a single semicircle. This merging suggests that the carrier density within all organic layers increases at higher voltages, reducing the relaxation time differences between the layers to a point where they become indistinguishable in the Cole-Cole plots. Similarly, in the Bode plots, the peak frequencies corresponding to each layer increase with voltage and eventually converge into a single peak. At high voltages (> 0.9 V), the single semicircle exhibits a slight distortion, as shown in Figure 3 (a) and (c). This distortion indicates an inhomogeneous carrier density distribution between the intrinsic and doped layers, reflecting partial differences in carrier dynamics.

After degradation, the Cole-Cole and Bode plots of both Devices A and B exhibit similar shapes, consistent with the trends observed in the earlier C-V measurements. In the Bode plots (Figure 3 (b) and (d)), the low-frequency peaks shift to higher frequencies, while the high-frequency peaks shift to lower frequencies. These opposing shifts reduce the relaxation time differences between the intrinsic and doped layers, leading to a shallower valley depth in the Cole-Cole plots. This behavior can be explained by two possible mechanisms: (1) the diffusion of p-dopants from the PCGL into the intrinsic layer, which increases the carrier density and conductivity of the intrinsic layer, causing the low-frequency peaks to shift to higher frequencies; or (2) improved interface injection due to heating, which also contributes to the shift of low-frequency peaks. Conversely, the shift of high-frequency peaks to lower frequencies is likely caused by the inter-diffusion of p- and n-dopants at the p-n interface. This inter-diffusion increases the resistance of the depletion and doped layers, resulting in the observed peak shifts.

3.3. Equivalent Circuit

With the aid of modulus spectroscopy, equivalent circuits of the CGU devices can be constructed, providing deeper insights into the degradation mechanisms. However, when using the equivalent circuit depicted in Figure 4 (a), the fitted curves fail to accurately replicate the measured curves (red dashed circle), indicating that the traditional equivalent circuit is insufficient. This imperfect fitting may arise from frequency-dependent conductivity as well as spatial inhomogeneities in dopant concentration within the doped layers.[4,9] Since the n-doped layer exhibits a depressed semicircle in the modulus spectrum, it is necessary to replace the capacitance with a constant phase element (CPE) to account for dispersive properties and achieve a more accurate model, as illustrated in Figure 4 (b).

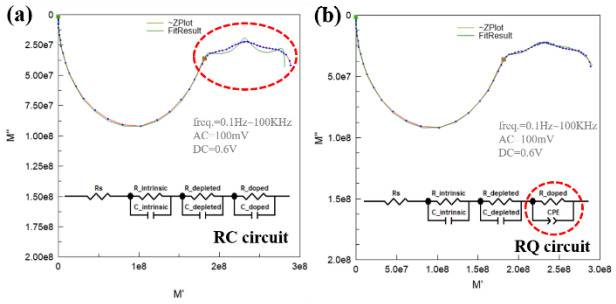

Figure 4. (a) Parallel resistance and capacitance (RC) and (b) parallel resistance and CPE (RQ) circuits with experimental data fitted to them.

The impedance of a CPE (Z_{CPE}) is defined as:

$$Z_{CPE} = \frac{1}{Q(j\omega)^{\alpha}}, \tag{4}$$

where ω is the frequency, Q is a frequency-independent parameter, and α is the CPE index ranging from 0 to 1. The interpretation of Q depends on the value of α and does not directly correspond to a specific physical quantity, except when $\alpha = 1$ (indicating a pure capacitance) or $\alpha = 0$ (indicating a pure resistance).[9] The effective capacitance (C_{eff}) can be derived using the formula:

$$C_{eff} = Q^{\frac{1}{\alpha}} R^{\frac{1}{\alpha}-1}. \tag{5}$$

The parameters (R, C and α) for the intrinsic, depleted and doped layers of both pristine and aged CGU devices, obtained from equivalent circuit fitting using the RQ circuit, are presented in Figure 5.

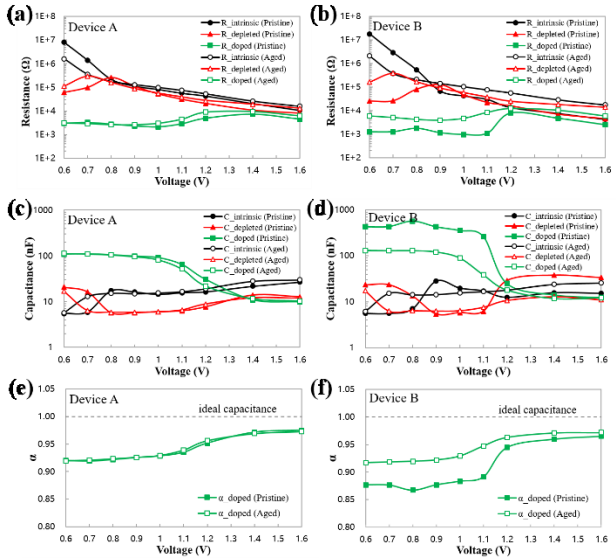

Figure 5. Variation of extracted circuit parameters as a function of bias voltage for (a), (c) and (e) Device A and (b), (d) and (f) Device B.

Figure 5 (a), (c) and (e) sequentially presents the resistance-voltage (R-V) plot, capacitance-voltage (C-V) plot, and CPE index α-voltage (α-V) plot of Device A before and after aging.

Similarly, the corresponding plots for Device B are displayed in Figure 5 (b), (d) and (f). Notably, due to the high carrier concentration in the doped layer, its resistance is several orders of magnitude smaller than that of the other layers, and its capacitance is also significantly higher than that of the other layers.

Focusing on the intrinsic layer (HTL), as the voltage increases, charges are generated at the doped p-n interface and subsequently transported to the intrinsic layer. This increased charge injection leads to a significant drop in resistance. Concurrently, the corresponding capacitance also rises due to the increase in carrier density.

In the case of the depleted layer, the resistance increases between 0.6 V and 0.8 V in the R-V plots, further confirming that the capacitance drop observed in the C-V curves is attributable to the widening of the depletion region thickness (W), as described by the formula $C=\varepsilon S/W$. As the voltage increases, electron tunneling in the depletion region becomes more effective, leading to a gradual decrease in resistance and a corresponding increase in capacitance.

Regarding the n-doped layer, Device B, with a 2.0 vol% Yb doping concentration, exhibits the most significant changes before and after aging. These changes are characterized by an increase in resistance, a significant reduction in capacitance, and a rise in the CPE index α. Such changes suggest that the primary cause of the increasing voltage shift is the diffusion of Yb dopants in the NCGL, which leads to a substantial decrease in carrier concentration. To mitigate this issue, a common approach is to insert an interlayer between the PCGL and NCGL. This interlayer plays a critical role in preventing chemical reactions or dopant inter-diffusion at the p-n interface, thereby enhancing device stability.[2]

4. Conclusion

The degradation of the CGL is primarily caused by dopant diffusion, particularly the diffusion of Yb atoms from the NCGL to the adjacent PCGL. This Yb diffusion induces impurity compensation, thereby increasing the driving voltage. Through C-V measurements and modulus spectroscopy, we visualized and validated changes in charge distribution within the aged CGL. Equivalent circuit fitting further quantified variations in resistance and capacitance, highlighting the significant impact of dopant diffusion on CGL performance.

5. References

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