A Wide-Data-Range Pixel Circuit for High-Pixel-Density Mobile Displays Using Double-Gate Oxide TFTs †

June-Hee Lee, Jin-Hyeong Kim, Hyeon-Ji Lee, Joo-Sun Lee, Byong-Deok Choi
Department of Electronic Engineering, Hanyang University, Seoul, South Korea

Abstract

For high-pixel-density mobile displays, the pixel current should be very low, which forces the driving transistor of the pixel to operate in the subthreshold region. In this region, the data voltage range becomes very narrow, making it very challenging to accommodate 10-bit data voltages. Additionally, this results in large current deviations. The proposed circuit, composed of four TFTs and two capacitors expands the data voltage range from 1.2V to 6.5V compared to the conventional pixel circuit. This improvement is achieved by controlling the bottom gate voltage of double-gate thin-film transistors (TFTs). The expansion of data voltage range also reduces the current deviation ratio from 150.9% to 71.7% when no compensation scheme is applied.

Author Keywords

AMOLED, high-pixel-density, pixel circuit, wide data range, current deviation, double-gate TFT

1. Introduction

Extensive research is being carried out on high-pixel-density OLED pixel circuits are being conducted. Particularly for application in the display panels of AR/VR devices[1][2]. These display panels for AR/VR devices are predominantly fabricated on silicon substrate (OLEDoS), which leads to significantly high production costs[3]. Alternatively, developing a high-PPI pixel circuit based on TFTs presents a promising solution for achieving substantial cost savings[4].

The luminance of OLEDs is determined by current density[5]. In high-PPI pixel circuits, the reduction in pixel area necessitates the circuit to output a very low driving current range. This low driving current range is achieved in the subthreshold region of the driving TFT, where the data voltage range becomes very narrow. As a result, implementing 10-bit grayscale becomes highly challenging, and the current becomes extremely sensitive to even small voltage variation. Consequently, current deviations caused by process variations such as V_{TH} shifts, become pronounced, leading to a significant reduction in luminance uniformity across the panel [6][7]. Therefore, expanding the data voltage range is strongly required to resolve these issues.

One approach that may seem straightforward for expanding the data voltage range is to increase the channel length of the driving TFT, However, a study has shown that in the subthreshold region, increasing the channel length of the driving TFT does not affect the data voltage range [2].

The proposed pixel circuit composed of four TFTs and two capacitors, expands the data voltage range by effectively controlling the back gate voltage of double-gate TFTs, thereby reducing the current deviation.

2. Proposed Pixel Circuit

Figure 1(a) illustrates the cross-sectional view of the double-gate TFT used in this study, featuring a four-terminal coplanar structure consisting of the source, drain, top gate, and bottom gate. Figure 1(b) presents the measured I_{DS}-V_{GS} characteristics with V_{BS} as a parameter. In this measurement, V_{DS} was fixed at 10 V, while V_{GS} was swept from -10 V to 10 V in 0.05 V increments. During the V_{GS} sweep, V_{BS} was fixed at specific values, varied from -5 V to 5 V in 1 V increments. It was observed that a positive V_{BS} shifts the curve to the left (negative shift), while a negative V_{BS} shifts it to the right (positive shift). This behavior also highlights that the drain current can be controlled by two independent voltages, V_{GS} and V_{BS}. To the best of our knowledge, previous studies on double-gate TFTs primarily focused on operating the bottom gate at either a fixed voltage or the same voltage as the top gate to achieve higher current levels [7][8]. For example, In Figure 1 (b), the blue line represents the drain current when V_{BS} is set to 0V. However, in this case, the subthreshold current slope is very steep, thus making the data voltage range significantly narrow.

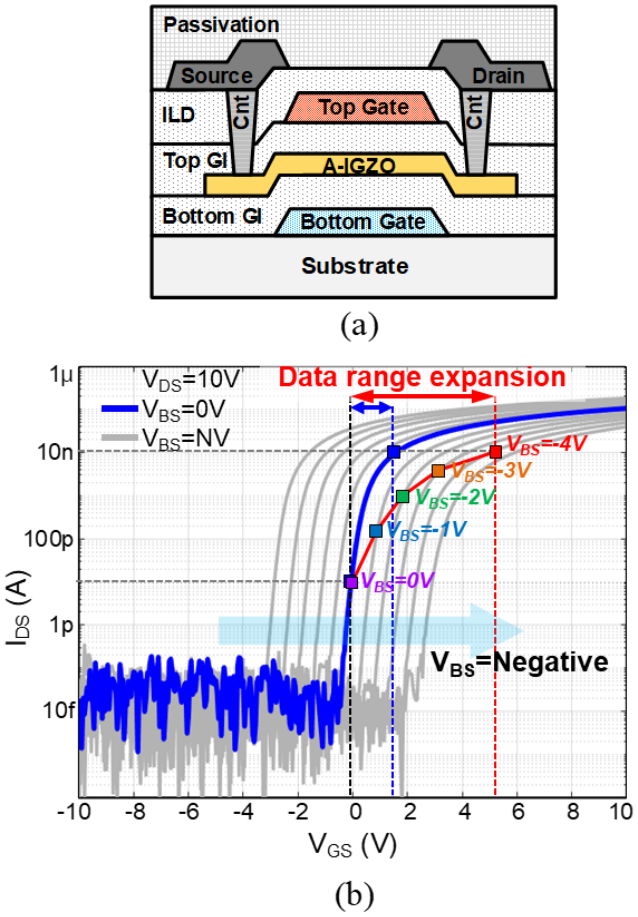

Figure 1. (a) The cross-sectional view of double-gate TFT, and (b) I_{DS}-V_{GS} characteristics of double-gate TFT.

ISSN 0097-996X/25/5603-1467-$1.00 © 2025

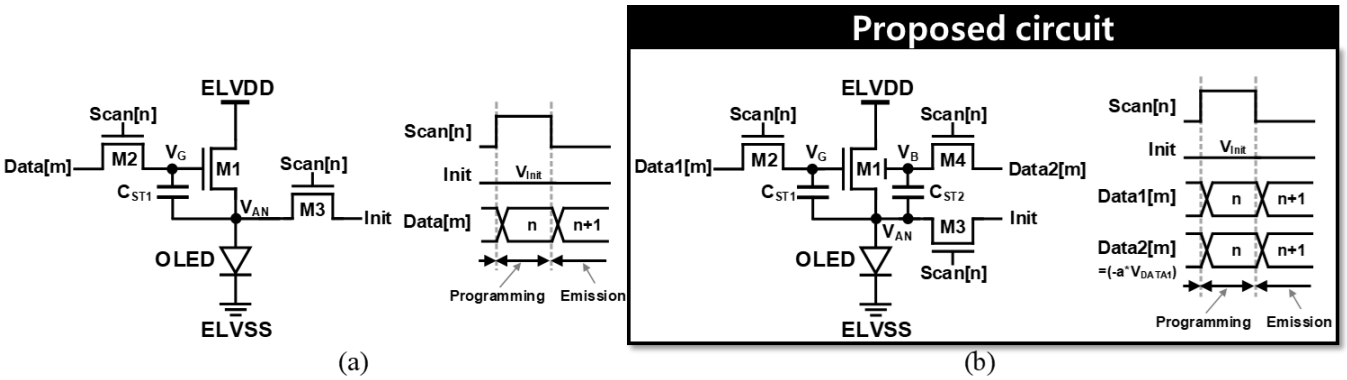

Figure 2. (a) Conventional 3T 1C pixel circuit, and (b) proposed 4T 2C bottom-gate controlled pixel circuit's schematic and timing diagram.

To expand the data voltage range, we focused on the fact that the drain current can be controlled by two independent voltages, V_{GS} and V_{BS}. As V_{GS} increases, V_{BS} is adjusted in the negative direction. This adjustment causes a positive shift in the curve, as illustrated in Figure 1(b). For example, by taking the red solid squares as bias points, the resulting I_{DS}-V_{GS} characteristics exhibit a gentler subthreshold slope, represented by the red line. This gentler slope effectively leads to an expansion of the data voltage range.

This phenomenon can be described using the current equation. In the subthreshold region, the relationship between the drain current of the double-gate TFT with the terminal voltages is expressed as

$$I_{DS} = I_0 \frac{W}{L} \exp\left(\frac{V_{GS} - V_{TH0} + \alpha(V_{BS})}{\eta V_T} \right) \quad (1)$$

where I_0, V_{TH0}, η, and V_T are the residual current, initial threshold voltage, subthreshold swing coefficient, and thermal voltage, respectively [9]. The current shift caused by V_{BS} is represented by $\alpha(V_{BS})$, where the coefficient α quantifies the extent of the I_{DS}-V_{GS} curve shift due to V_{BS}. This coefficient is determined by the capacitance of the top gate and bottom gate[9][10][11]. As the data voltage, which defines V_{GS}, increases, the drain current increases. However, by appropriately applying negative V_{BS} voltages, the increase in drain current can be suppressed, resulting in positive shifts in the I_{DS}-V_{GS} characteristics. To implement this concept, a pixel circuit composed of four TFTs and two capacitors (4T 2C) is proposed. For comparison a conventional 3-TFT, 1-capacitor pixel circuit is also introduced.

(a) 3T 1C conventional pixel circuit: Figure 2(a) illustrates the schematic and timing diagram of a conventional pixel circuit implemented using single-gate oxide TFTs. The circuit consists of a driving TFT (M1), a switching TFT (M2) connected to the gate node (V_G), another switching TFT (M3) for initializing the anode of the OLED (V_{AN}) and a storage capacitor (C_{ST1}). During the programming period, Scan[n] is high, V_G=V_{DATA} and V_{AN}=V_{INIT}, allowing data programming. During the emission period, the pixel outputs the driving current.

(b) Proposed 4T 2C bottom-gate controlled pixel circuit: Figure 2(b) presents the schematic and timing diagram of the proposed pixel circuit, which employs a double-gate oxide TFT as the driving TFT. In this design, the bottom-gate is connected to Data2[m] via a switching TFT (M4), and a storage capacitor is placed between V_B (the bottom-gate voltage) and V_{AN} (the anode voltage of the OLED). During the programming period, V_G receives V_{DATA1} through Datat1[m], V_B receives V_{DATA2} through Data2[m], and V_{AN} is set to V_{INIT}. In the emission period, all switching TFTs are turned off, and the driving TFT outputs the programmed emission current. In this circuit, V_{DATA2} designed to be negatively proportional to V_{DATA1}, resulting in positive shifts in the emission current, effectively expanding the data voltage range.

3. Measurement results

The proposed circuit was fabricated using a minimum 3 μm-length oxide TFT backplane process. Table 1 presents the component dimensions for both the conventional and proposed pixel circuits. The switching and driving TFTs in the (a) conventional 3T 1C circuit and the (b) proposed 4T 2C circuit were designed with a minimum W/L of 3 μm /3 μm. While increasing the length of the driving TFT could barely expand the data voltage range, it also increases the pixel area, which is undesirable for high-density displays. Therefore, the driving TFT was designed with the minimum size to maximize the pixel density. As a result, the conventional circuit has a resolution of 888-PPI, and the proposed circuit has 703-PPI, as shown in Figure 3.

Table 1. The dimensions of pixel circuit's components

Design parameter	(a)	(b)
W/L of TFTs	3μm/3μm	3μm/3μm
C_{ST1}	17.7fF	10.2fF
C_{ST2}	-	9.9fF
PPI	888-PPI	703-PPI

Table 2. Measurement conditions.

Design parameter	Value
Frequency	370kHz
ELVDD	8V
ELVSS	0V
V_{INIT}	0V
Scan[n]	-6V ~ 10V

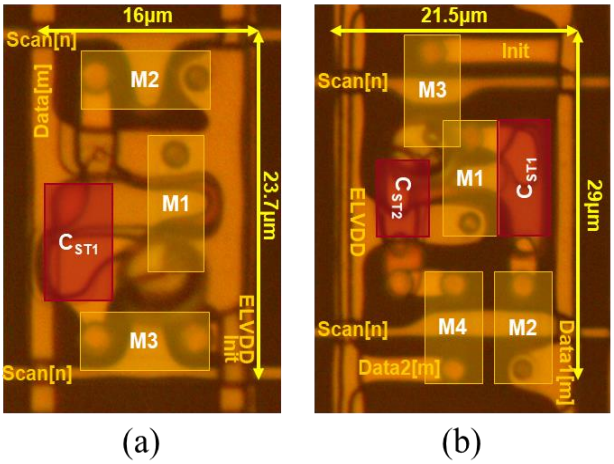

Figure 3. Micrographs of (a) conventional 3T 1C pixel circuit, and (b) proposed 4T 2C bottom-gate controlled pixel circuit.

Table 3. Measurement results

Pixel circuit	V_{DATA2} condition	Data range (rate of change)	Max. current deviation
(a) 3T 1C	-	1.20V (-%)	150.9%
(b) Proposed 4T 2C	V_{DATA2}=-0.1V_{DATA1}	4.25V (354%)	90.7%
	V_{DATA2}=-0.5V_{DATA1}	6.50V (542%)	71.7%

The circuit operation was verified through measurements under the conditions listed in Table 2. The measurement setup included a probe station (MT5500B), a picoammeter (B2983B), a function generator(33500B), and a power supply(2233G-30-1).

Figure 4(a) presents the measurement results for the conventional 3T 1C pixel circuit. For a driving current range of 10 pA to 10 nA, the average data range for the measured 5 samples was 1.2 V. The maximum current deviation from the average current, was 150.9% as shown in Figure 4(c). Figure 4(b) presents the measurement results for the proposed 4T 2C bottom-gate controlled pixel circuit. This circuit expands the data range by modifying V_{DATA2}. Measurements were taken at $V_{DATA2}=-0.1 \cdot V_{DATA1}$ and $V_{DATA2}=-0.5 \cdot V_{DATA1}$. The data ranges for producing the same driving current range were measured as 4.25 V and 6.5 V, respectively. The maximum current deviations from the average currents were 90.7% and 71.7%, respectively, as shown in Figure 4(c). Compared to the 3T 1C conventional pixel circuit, the data ranges increased by 4.25 V and 6.5 V, and the maximum current deviations decreased by 60.1% and 79.2% respectively.

These measurement results confirm that the proposed circuit effectively expands the data range compared to the conventional 3T 1C pixel circuit and the current deviation is reduced.

4. Conclusion

In high-pixel-density displays, the reduction in pixel driving current causes the driving TFT to operate in the subthreshold region. In this region, the data voltage range becomes narrow, and the driving current becomes highly sensitive to variations in the data voltage, leading to significant current deviations due to these variations.

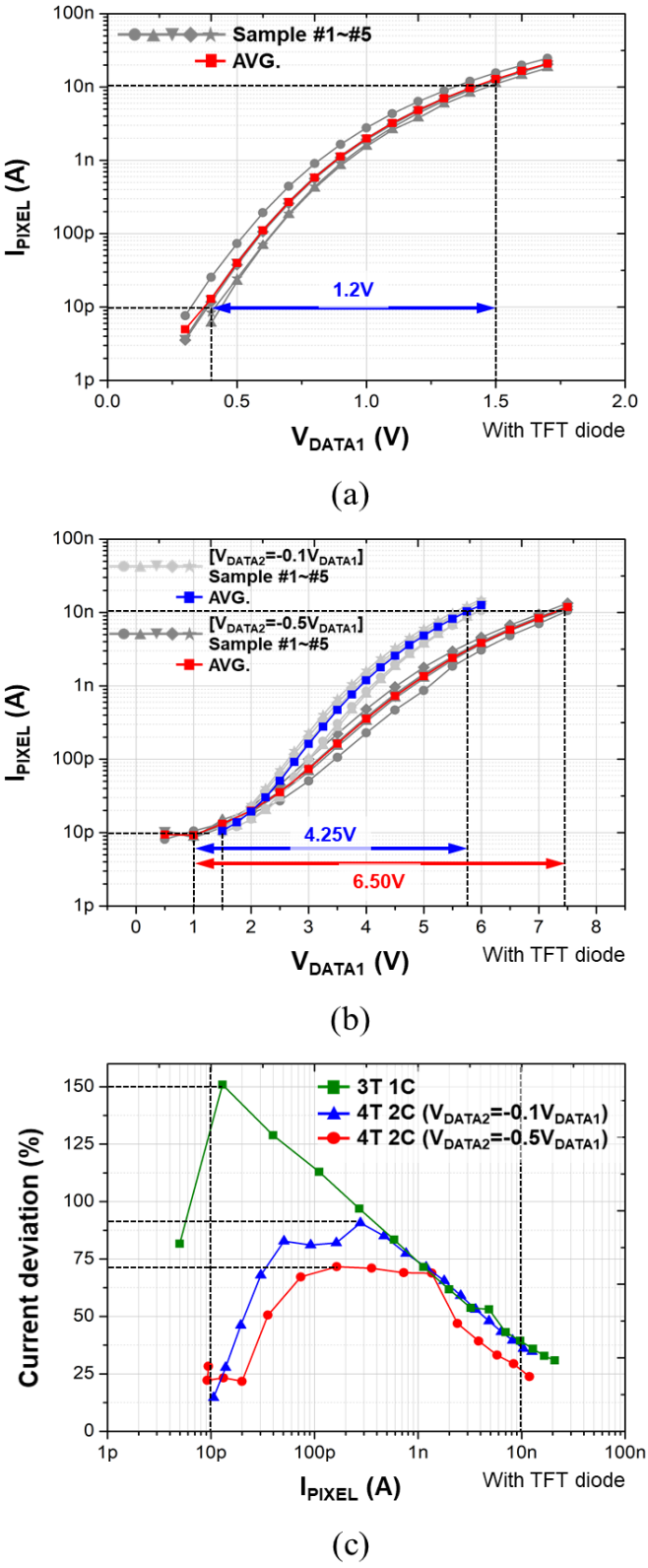

Figure 3. (a) Conventional 3T 1C pixel circuit, (b) proposed 4T 2C bottom-gate controlled pixel circuit's data voltage ranges, and (c) comparison of current deviation between 3T 1C and 4T 2C pixel circuits.

The proposed circuit addresses this issue by utilizing a double-gate TFT as the driving TFT. By employing double-gate control, the data voltage range is significantly expanded, which in turn reduces current deviation. A comparison between the proposed circuit and the conventional pixel circuit was conducted, focusing on data range, and driving current deviation. The proposed circuit expands the data voltage range from 1.2 V to 6.5 V, a significant improvement over the conventional pixel circuit. Moreover, the maximum current deviation was reduced from 150.9% to 71.7%.

5. Acknowledgements

This work was supported by the Technology Innovation Program (Project Number. 20016317 Project Name. On-panel circuit integration and driving system technology for 1270 ppi low-power OLED display based on oxide semiconductor') funded by the Ministry of Trade, Industry & Energy (MOTIE, Korea)

The EDA tool was supported by the IC Design Education Center (IDEC), Korea.

6. References

[1] Cheng, S.-S. and P. C.-P. Chao (2024). "An Ultra-High 6318-PPI Pixel Circuit for Micro-OLED Displays With V_{TH} Compensated up to 10-bit Gray Levels." IEEE Journal of Solid-State Circuits.

[2] Shin, H. J., et al. (2024). "4670-PPI OLEDoS pixel circuit design for wide data voltage range in a 5 V 0.13 μm CMOS process." Journal of the Society for Information Display.

[3] Kwak, B.-C. and O.-K. Kwon (2016). "A 2822-ppi resolution pixel circuit with high luminance uniformity for OLED microdisplays." Journal of Display Technology 12(10): 1083-1088.

[4] Na, J.-S., et al. (2019). "A 4410-ppi resolution pixel circuit for high luminance uniformity of OLEDoS microdisplays." IEEE Journal of the Electron Devices Society 7: 1026-1032.

[5] Geffroy, B., et al. (2006). "Organic light-emitting diode (OLED) technology: materials, devices and display technologies." Polymer international 55(6): 572-582.

[6] Keum, N.-H., et al. (2018). 23-1: Distinquished Student Paper: An AMOLED Pixel Circuit for 1000 ppi and 5.87-inch Mobile Displays with AR and VR Applications. SID Symposium Digest of Technical Papers, Wiley Online Library.

[7] You, Y., et al. (2024). "Double-gate metal–oxide TFT pixel circuit for improved luminance uniformity of mobile OLED display." Journal of Information Display: 1-9.

[8] Lee, J., et al. (2020). "Organic light-emitting diode display pixel circuit employing double-gate low-temperature poly-Si thin-film transistor and metal-oxide thin-film transistors." Journal of the Society for Information Display 28(12): 1003-1011.

[9] Abe, K., et al. (2012). "Amorphous In–Ga–Zn–O dual-gate TFTs: Current–voltage characteristics and electrical stress instabilities." IEEE Transactions on Electron Devices 59(7): 1928-1935.

[10] Seok, M. J., et al. (2011). "A full-swing a-IGZO TFT-based inverter with a top-gate-bias-induced depletion load." IEEE electron device letters 32(8): 1089-1091.

[11] Baek, G., et al. (2011). "Electrical properties and stability of dual-gate coplanar homojunction DC sputtered amorphous indium–gallium–zinc–oxide thin-film transistors and its application to AM-OLEDs." IEEE Transactions on Electron Devices 58(12): 4344-4353.