Multi-Frequency Gate Driver in the Controllable Region for Low Power TFT-LCD Application

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Abstract

In this paper, a gate driver circuit using amorphous silicon (a-Si) thin-film transistors (TFTs) is proposed. It blocks the output signals and controls the refresh rate 60Hz to 1Hz in multiple regions of the panel which are selected. Simulation results show that the proposed circuit can be operated at extreme environment power consumption can be reduced in proportion to the decrease in frequency.

Author Keywords

Gate driver on array; Amorphous silicon (a-Si); Thin film transistor (TFT); Multi-frequency; Low power consumption.

Introduction

Amorphous silicon thin-film transistors, known as a-Si TFTs, have become widely used in the TFT-LCD market due to their low cost, excellent uniformity, and mature manufacturing technology [1-2]. In the present era, display technology has become an integral part of daily life, extensively utilized in smartphones, notebooks, tablets, and portable devices. As the demand for high-tech electronic products grows, the design of display panels must be lighter, thinner, and more cost-effective. High refresh rate provides better image quality and smoother visuals during dynamic scenes, but it also increases power consumption.

To achieve both high performance and efficient power consumption, a new driving method has been introduced to optimize both performance and power efficiency by adjusting the refresh rate based on display content [3]. The required refresh rate varies with the user's activity. For instance, a higher refresh rate, at least 60Hz or above, is necessary for gaming or movies. However, for web browsing or static content, a refresh rate below 30Hz is adequate. Therefore, a higher refresh rate is not always preferable in every situation [4]. Fig. 1. illustrates a method for applying low frequency driving by masking input data frames [5]. The original output frequency of the gate driver is 60Hz. When even frames are masked, the display is operated at 30Hz.

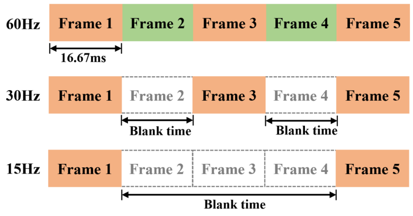

Fig 1. The driving method for masking frames. [5]

Although reducing the frequency can effectively save power for full-screen frequency reduction, partial-area frequency reduction not only maintains the benefits of energy saving but also provides different corresponding frequencies based on the frequency requirements of different areas, without affecting the viewer's experience of the image.

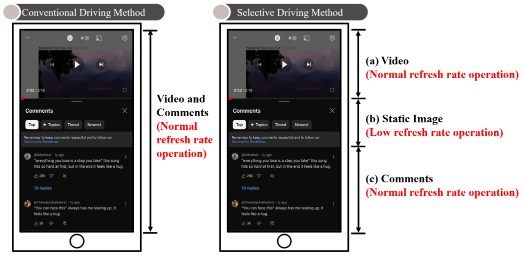

Fig 2. A schematic diagram of conventional driving and the proposed selective scan driving.

Considering the idea of the partial-area frequency reduction, this article proposes a new gate driver circuit with multi-frequency in the selected regions for TFT-LCDs. As shown in Fig. 2, the proposed circuit maintains the original refresh rate in the videos and comments regions while it reduces the refresh rate in the static image regions. This approach minimizes the unnecessary power consumption and balances the energy efficiency with a high-quality visual experience.

Operation of the proposed gate driver

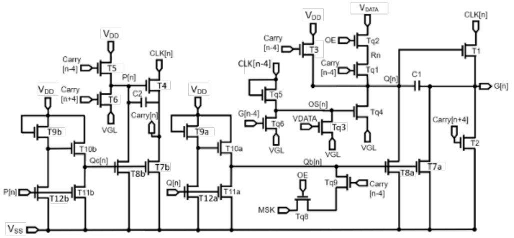

Fig 3. The driving scheme of the proposed gate driver.

Fig. 3 presents the circuit schematic of proposed gate driver. The circuit can be divided into five blocks, which are selective driving block, noise-free block, carry-stage block, pre-charging block, and driving block. There are three additional signals for the proposed selective driving block. OE signal determines whether the pre-charging node (Q[n]) of the gate driver is charged or not. VDATA is used as the start signal for the arbitrarily selected area. MSK is responsible for activating the noise-free node (Qb[n]) to blocks output signal. The block diagram for one stage of the proposed gate driver circuit is shown in Fig. 4(a), which is consisted of the input signals (G[n-4], Carry[n-4], and Carry[n+4]), control signals (CLK1~ CLK8), two output signals (G[n] and Carry[n]), and additional signals (OE, VDATA, MSK).

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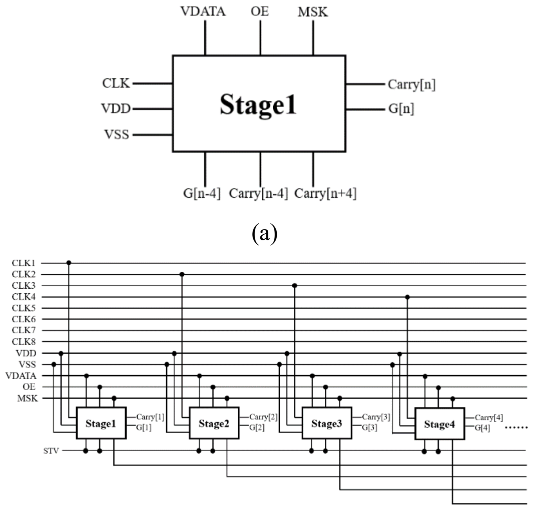
The voltage of VDD and VSS are15V and -12V, respectively. The detailed connections for each stage are shown in Fig. 4(b).



(a)

(b)

Fig 4. (a) The block diagram of one stage for the proposed circuit and (b) The detailed connection between each stage of the gate driver circuit.

The carry-stage block of the proposed circuit serves two functions as it does not reduce frequency such as the output signal G[n]. The first function is to replace G[n] as the pre-charge and pull-down signals for subsequent stages, which decreases the RC loading of the G[n]. The second function is to define the frequency reduction regions with OE, determining when Q[n] discharges and recharges.

The timing diagram of the proposed circuit is shown in Fig. 5. The proposed gate driver circuit operates in the following seven periods. It represents an example of blocking six stages (G[n]–G[n+5]) selectively. The operation principle is described as follows:

Firstly, in the period (1) for programming period, Carry[n-4] is at a high voltage level, causing T3 and T5 to open, charging Q[n] and P[n] to VDD-Vth, T3 and VDD-Vth, T5. Since T3 and T5 is opened and CLK is at a low voltage level, G[n] and Carry[n] output low voltage level. The signal OS[n] is at a high voltage in this period.

Next is a period (2), Q[n] node and P[n] node maintained at a high voltage level. As CLK transitions from VDD to VSS, the Q[n] node is bootstrapped by C1 and T1, and P[n] node is bootstrapped by C2 and T4. Thus, the driving capability of T1 and T4 are increased, and the high voltage of CLK is stably transmitted to G[n] and Carry[n].

In the period (3), CLK[n-4] becomes VDD and G[n-4] is at a low voltage level, causing Tq5 to turn on and Tq6 to turn off, respectively. Therefore, OS[n] node becomes high voltage through Tq5 to turn on Tq4, which leads to the discharging of Q[n] node. Simultaneously, Carry[n+4] is at a high voltage so that T2 and T6 are turned on to pull down G[n] and P[n] to a low voltage level.

In the period (4), since the discharging of the Q[n] node and P[n] node, T11a, T11b, T12a and T12b are turned off. Qb[n] node and Qc[n] node become high voltage level. As a result, G[n] will maintain VSS voltage through T7a, and Carry[n] will maintain VSS voltage through T7b to achieve noise-free when the proposed circuit is operated at a non-working period.

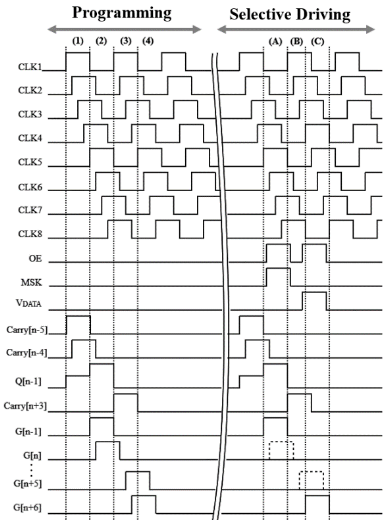


Fig5. The timing diagram of the proposed gate driver.

In period (A) for selective driving period in the next frame, VDATA is at a low voltage level. Since both the OE signal and Carry[n-4] are at a high voltage level, Tq1 and Tq2 are turned on. With VDATA at a low voltage level, Q[n] is discharged to a low voltage level through the discharging path of Tq1 and Tq2. This causes a pre-charge failure at Q[n] in the first stage for the frequency reduction. Therefore, the circuit does not enter the working period. Meanwhile, Tq8 and Tq9 are turned on, and MSK is at a high voltage level, charging Qb[n], which activates the noise-free TFTs T7a and T8a to help pull down Q[n], preventing G[n] from outputting noise.

In the next period (B), when the output node of the preceding stage is absent, G[n-4] is at a low voltage level and Tq6 is turned off. CLK[n-4] is at a high voltage level so that OS[n] is charged to a high voltage level, activating Tq4 to pull down Q[n] at the intermediate stages for frequency reduction region. Thus, the function of OS[n] block is to create additional discharging path, preventing OE from maintaining at a high voltage for a long time and causing the degradation of Tq2.

Finally, there is the period (C), with both OE and VDATA at a high voltage level, Tq1 and Tq2 are turned on, charging Q[n] to a high voltage. Since VDATA is high, OS[n] is pulled down to a low voltage level, turning off Tq4. Meanwhile, MSK is at a low voltage level, which turns off the noise-free TFTs T7a and T8a, allowing Q[n] to successfully recharge. Consequently, G[n] can output a high voltage level during the working period.

Experiment result and discussion

The proposed gate driver circuit is designed and simulated using "SmartSpice." The a-Si TFT model utilized in this paper was developed using the fitting EDA tool "Utmost" at level = 35. Table 1 shows the aspect ratios of the TFT devices and the voltage range of the signal lines used in the proposed circuit. The input signals include a high voltage VDD of 15V, a low voltage VSS of -12V, and a combination of control signals (OE, VDATA, and MSK), which select gate lines with a lower refresh rate during the selective driving period. Additionally, the circuit includes a start pulse (STV), a stop pulse (STP), and eight clock signals (CLK1~CLK8). The circuit will be simulated at temperatures of

25°C, 85°C, and -40°C to verify its functionality.

Table 1. Design parameters of the proposed gate driver circuit.

TFT#	W/L(μm/μm)	TFT#	W/L(μm/μm)
T1	3000/3.5	Tq1, Tq2	600/3.5
T2~T7	300/3.5	Tq3, Tq4	300/3.5
T8a, T8b	50/3.5	Tq5	50/3.5
T9a, T10a	100/3.5	Tq6, Tq7	300/3.5
T9b, T11a	300/3.5	Tq8, Tq9	600/3.5
C1	1pF	C2	1pF
W = Channel Width, L = Channel Length			
Voltage of signal lines			
V_{DD}	15V	V_{SS}	-12V
CLK	-12V~15V	OE	-12V~15V
V_{DATA}	-12V~15V	MSK	-12V~15V

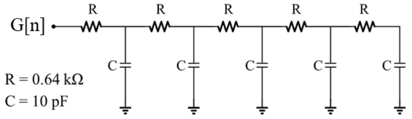


Fig 6. Gate-line loading of the scan driver circuit.

As shown in Fig. 6, the RC loading of the panel is 3.2 KΩ and 50 pF, respectively, and the input voltage range is from -12V to 15V. To verify the functionality of the proposed circuit, Fig. 7 presents the simulation results of the OE signal and the output nodes G[n] at 25°C. The first frame was set to operate normally without frequency reduction. In the second frame, the region from G[7] to G[16] was selected for frequency reduction. The simulation results were successful, with no output signals transmitted from G[7] to G[16] to the gate lines, while the stages after G[16] continued to transmit pulse signals normally. This effectively reduced the frequency for the middle 10 stages. The performance of the proposed GOA circuit, including rise time, fall time, and noise RMS values, is summarized in Table 2. The rise time is measured from 10% to 90% of the voltage difference between VSS (-12V) and VDD (15V), while the fall time is measured from 90% to 10% of the same voltage difference. The noise RMS is calculated as the root mean square value of the output node during the non-working period.

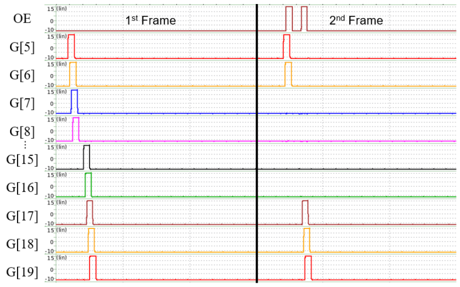


Fig 7. Simulated waveforms of the OE signal and the output nodes at 25℃.

The reliability of the proposed gate driver circuit under wide temperature conditions is also crucial. Therefore, the circuit was simulated at both high (85°C) and low (-40°C) temperatures. Figures 8 and 9 show the simulation results of the OE signal and the output nodes G[n] at 85°C and -40°C, respectively. At high temperatures, due to the hot carrier effect, the rise time and fall time are faster compared to room temperature. At low temperatures, electron mobility decreases, which may slow down the charging and discharging rates. To address the challenges of a-Si TFTs operating at low temperatures, a clock overlapping method was implemented to extend the pre-charging time. Tables 3 and 4 present the rise time, fall time, and noise RMS values at 85°C and -40°C, respectively.

Table 2. Simulation Results of the OE signal and the output nodes at 25℃.

Simulation results at 25°C			
	Rising Time (μs)	Falling Time (μs)	RMS (V)
1st Frame			
G6	2.93	2.59	0.008
G17	2.92	2.58	0. 008
G18	2.92	2.58	0.008
2nd Frame			
G6	2.96	2.63	0.008
The operation of blocking 10 stages (G7 to G16)			
G17	3.07	2.67	0. 008
G18	2.85	2.49	0.008

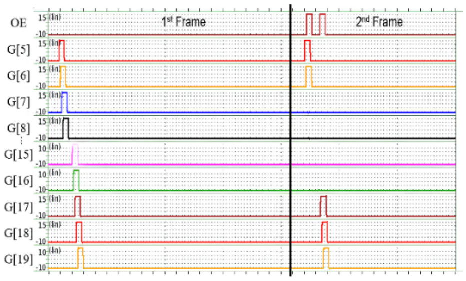


Fig 8. Simulated waveforms of the OE signal and the output nodes at 85℃.

Table 3. Simulation Results of the OE signal and the output nodes at 85℃.

Simulation results at 85°C			
	Rising Time (μs)	Falling Time (μs)	RMS (V)
1st Frame			
G6	2.32	4.25	0.050
G17	2.37	4.32	0. 048
G18	2.37	4.32	0.047
2nd Frame			
G6	2.33	4.78	0.048
The operation of blocking 10 stages (G7 to G16)			
G17	2.09	3.69	0. 049
G18	2.15	3.82	0.048

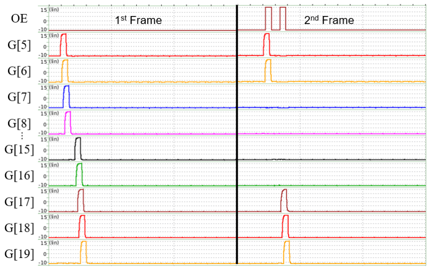


Fig 9. Simulated waveforms of the OE signal and the output nodes at -40℃.

Table 4. Simulation Results of the OE signal and the output nodes at -40℃.

Simulation results at-40°C			
	Rising Time (μs)	**Falling Time (μs)**	**RMS (V)**
1st Frame			
G6	16.47	8.39	0.031
G17	16.45	8.27	0. 031
G18	16.46	8.28	0.030
2nd Frame			
G6	16.50	8.49	0.031
The operation of blocking 10 stages (G7 to G16)			
G17	26.12	12.38	0. 031
G18	16.35	8.34	0.030

Furthermore, Fig. 10 shows the simulation results from G[5] to G[23] at 25°C. The refresh rate is set at 30Hz from G[7] to G[11], and it is noticed that the even frames are masked, which is the first frequency reduction region. Then, the region from G[12] to G[16] maintains the original refresh rate of 60Hz. In the second frequency reduction region, the refresh rate for the region from G[17] to G[21] is set to drop to 15Hz, where it is observed that the second and third frames are masked. Finally, the region from G[22] to G[23] maintains the original refresh rate of 60Hz. Therefore, the proposed GOA circuit offers the flexibility to select multiple regions for frequency reduction, and it can be applied to various display contents.

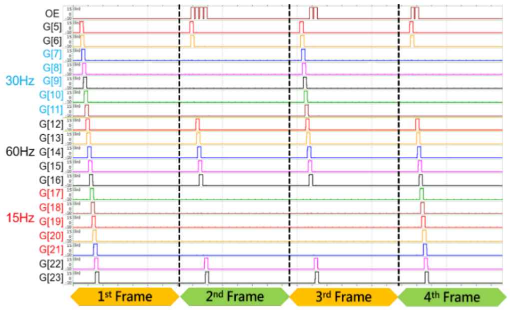


Fig 10. Simulated waveforms of the output nodes at the refresh rate of 60Hz, 30Hz, and 15Hz.

Finally, the discussion on dynamic power consumption is presented in Table 5. The power consumption generated on gate lines can be calculated with the equation (1). According to the given specifications, the total equivalent capacitance of the liquid crystal on a gate line is estimated to be approximately 11.57nF [6]. Therefore, the dynamic power consumption of 720 gate lines at different frequencies can be calculated. Furthermore, the dynamic power consumption of the GOA circuit is also simulated by SPICE tool. The first condition is the original refresh rate of 60Hz. In the first case, the total dynamic power consumption on the gate lines is 364.37mW, while the power consumption of the 720-stage GOA circuit is 15.614mW. In the second condition, the refresh rate for one-third of the whole region is 30Hz while the other two-thirds is 60Hz. In this case, the total dynamic power consumption on the gate lines is 303.64mW, while the power consumption of the 720-stage GOA circuit is 16.078mW. In the third condition, the refresh rate for one-third of the whole region is reduced to 1Hz while the remaining two-thirds is 60Hz. Under this condition, the total dynamic power consumption on the gate lines is 244.93mW, while the power consumption of the 720-stage GOA circuit is 17.873mW. It is found that the addition of the control signals OE, VDATA, and MSK increases the power consumption of the gate driver circuit. Nevertheless, the overall reduction in dynamic power consumption is still significant. Therefore, by reducing the refresh rate in regions which do not require high refresh rate, the unnecessary power consumption can be saved.

Table 5. The dynamic power consumption of gate lines and GOA circuit under different display conditions.

	Gate lines (Calculation)	GOA circuit (Simulation)	Overall Reduction
Normal refresh rate (60Hz)	364.37 mW	15.614 mW	-
60Hz in 2/3 region 30Hz in 1/3 region	303.64 mW	16.078 mW	-60.27 mW
60Hz in 2/3 region 1Hz in 1/3 region	244.93 mW	17.873 mW	-56.92 mW

Conclusion

A multi-frequency gate driver in the selected regions has been proposed. The circuit utilizes additional OE, MSK, and VDATA signals to achieve multi-frequency in the selected regions. Furthermore, the carry-stage not only reduces the loading observed at the output but also cooperates with OE to determine the beginning and end of the frequency reduction region. This allows the display to selectively choose multiple regions and multiple stages for frequency reduction. Therefore, with the reduction of the refresh rate in the unnecessary regions, it is possible to save wasted power consumption. Simulation results demonstrate that multi-region frequency reduction can be achieved, and the circuit operates successfully at 25°C, 85°C, and -40°C which supports the focus on green energy development nowadays.

Acknowledgements

This work was supported by the National Science and Technology Council (NSTC), Taiwan, under NSTC 113-2218-E-A49 -019 –MBK, 113-2218-E-A49-021-MBK, 112-2221-E-A49 -132 -MY3, and NSTC T-Star Center Project: Future Semiconductor Technology Research Center under NSTC 111-2634-F-A49-008-. Also supported in part by the Advanced Semiconductor Technology Research Center under Higher Education Sprout Project of Ministry of Education, Taiwan, as well as by Giantplus Technology Corporation, Taoyuan, Taiwan.

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