Femto-Ampere Leakage Current of Low Temperature Poly-Silicon TFTs in OLED Panel†

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Abstract

A few Femto-amperes off leakage current was confirmed with Low Temperature Poly-Silicon TFTs in OLED Panels by TFT aging method. Since its use in flat panel displays, LTPS TFTs have not been considered to have low off leakage below pico-amperes because of the grain boundaries defects known as the origin. However, in this paper, it was confirmed that ELA LTPS TFTs can have the value of a few fA, which is the lower leakage current than Single Crystalline Si device [1].

Author Keywords

Femto-Ampere; LTPS; Thin Film Transistors; OLED.

1. Introduction

Since flat panel display appeared in Information Technology, Low Temperature Poly Silicon (LTPS) Thin Film Transistors (TFTs) have been a great role in the panel for LCD and OLED display. [2] As well known, it has moderate mobility and good reliability for display application, but off-leakage characteristics have been considered relatively insufficient compared to a-Si or oxide TFTs. Due to the idea that LTPS would have relatively high off-leakage, LTPS TFT has not been accepted to implement low frequency driving, yet. Therefore Low Temperature Polysilicon Oxide (LTPO) technology was developed and being used for low frequency driving in OLED panel, which is cutting-edge technology in the display area at this moment. For the time being, LTPO will be adopted for low frequency driving. However, due to the low mobility and the instability of Oxide TFTs compared to LTPS, it makes difficulties to construct small size of driving circuits in bezel area and low driving voltage for power consumption. Since LTPO technology contains two different semiconductor materials, it leads to complex process architectures and high costs in OLED panels.

In this paper, we present leakage current of a few femto amperes with experimental results of PMOS LTPS TFTs. To reduce Gate Induced Drain Leakage (GIDL) current, off aging process was applied to the TFTs. Also, a relationship between leakage and subthreshold swing was reviewed with experiments.

2. Theoreitcal Background

The causes of leakage currents in transistors are considered to have three components consisted of thermionic emission (TE), thermionic field emission (TFE) and field emission (FE). [3] The thermionic emission is linearly dependent on given temperature and the field emission can be appeared in tunneling, which is known as charge penetration through energy barrier. The leakage current by tunneling phenomenon is related to the field between gate and drain in a transistor in the strong inversion region, which known as GIDL. An example of GIDL is shown in Figure 1. Except those mechanisms, defects and grain-boundaries are specific factors to accelerate leakage current further. Since the defect as a trap charge, such as dangling bond of silicon, always exists in the active vicinity, therefore trap-assisted thermal emission and trap-assisted tunneling occur in common. In addition, poly-Si has grain-boundaries, which is well-known for a cause of mobility decrement because of a role for energy barrier, which has effect to interrupt charge transfer. And as the result, charge through GBs decrease, which cause not only on-current decrease, but also off-current decrease. This is important that can explain LTPS TFTs can have low off-leakage current.

In this work, off leakage in LTPS TFTs was intensively investigated both in theory as well as experiments. [4, 5, 6] In Figure 1 TE current is denoted as G, TFE current is denoted as T1 and FE current is denoted as T2, respectively. Regions in depletion width that G, T1 and T2 occurred are denoted as W, W_{T1} and W_{T2}. In the case of p-type LTPS TFTs, when high positive gate bias and negative drain bias are applied, channel and drain junction are under reverse bias (see Figure 1). Under the reverse bias, the bandwidth become narrower and it makes easier for tunneling process. Therefore, the GIDL is intensively attributed trap-assisted-tunneling (TAT) processes, and further accelerated by the traps, which is defects in grain boundary and interface of polysilicon in the TFTs. Also, TAT current can be further divided into thermionic field emission (TFE) and field emission (FE).

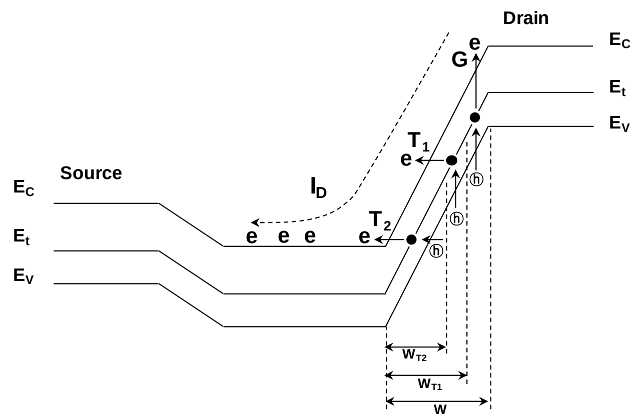

Figure 1. Band diagram of trap-assisted leakage current and its component in LTPS TFTs.

3. Experimental Setup

For fabriacation of LTPS TFTs, the ELA crystallization method was applied for LTPS TFT production, and the top gate's coplanar structure was adopted. Molybdenum was used as the gate metal, and a PECVD SiOx thin film was used as the gate insulator. For low off current measurement setup, an Agilent B1500 semiconductor parameter analyzer was connected directly with probe-tips. The connecting cables are low resistance tri-axial cables with the minimum length and the probe tips are low resistance type (DCP120). All of measurements were conducted in a dark, metal-shielded chamber, which was placed on a vibration proof stage. Integration time and source-monitor-unit range setting were set as PLC16 and 1E-11 respectively that

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enables 1fA resolution according to B1500A specification. Transfer characteristics were measured with gate bias (V_G) within ±15V, drain bias (V_D) was -5.1V, and source bias (V_S) grounded. Off aging was conducted at grounded source and gate while drain bias was set at specific bias.

4. Results & Discussion

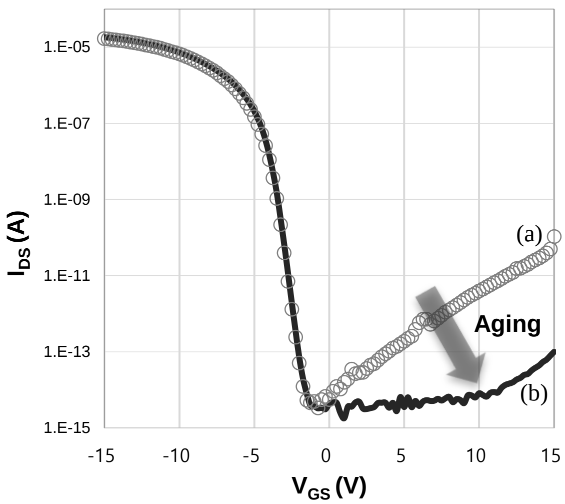

Figure 2. Reduction of GIDL by aging process on LTPS TFTs. Minimum off current is found at V_{GS} 1V. Two Transfer curves compared with (a) before aging and (b) after aging

In the OLED backplane process for LTPS TFTs, it is confirmed that femto ampere off current are realized in the product. Figure 2 shows that off leakage can be suppressed to the femto amperes after aging process. These results imply that even if there are defects in poly-Si, leakage due to tunneling is suppressed to the femto ampere level due to charge injection into gate insulator nearby gate to drain edge. When injected charges are clustered, they would act like an electrode to shield the field between gate and drain.

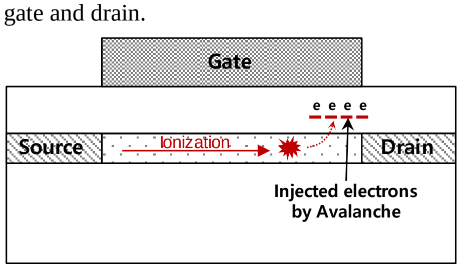

Figure 3. Schematic of electron charge injection to Gate-Drain edge by avalanche ionization during aging process

The aging is the process for a TFT to reduce the GIDL current. As shown in Figure 3, when a large enough electric field is placed between source and drain of TFTs, the charge in the channel accelerates under an electric field, and as a result, it collides with another charge and ionizes it. This phenomenon is called impact ionization or avalanche ionization. The ionized charge is embedded in an insulator at the drain end of the TFT, and these charges gather to serve as an electrode to block the gate field. As the results of aging process, the off current could reach to femto-ampere level. As shown in Figure 2, it can be seen that the GIDL current before aging decreases rapidly after aging.

This aging effect is expected to reduce not only GIDL but also the leakage by thermionic emission. When considered the G.B potential barriers in the channel through current path, G.B barrier can be lowered with positive gate voltage, which result in current increase of thermionic emission leakages. However, if there is injected charge shield in the insulator at the drain edge, it blocks gate field to G.Bs and G.Bs potential height could be maintained. This operation bring to suppress the thermionic emission leakage into drain. In these G.Bs characteristics, poly-Si TFTs has lower mobility and leakage than c-Si, which shows con and pro in device performance.

Figure 4 and 5 show representative LTPS TFT characteristics and correlation between off current and drain bias, respectively. It can be seen that the lower the V_{DS} in the off section of the transfer curve, the smaller the GIDL appeared. From these results, it can be assumed that the drain voltage plays a major role as the cause of generating GIDL.

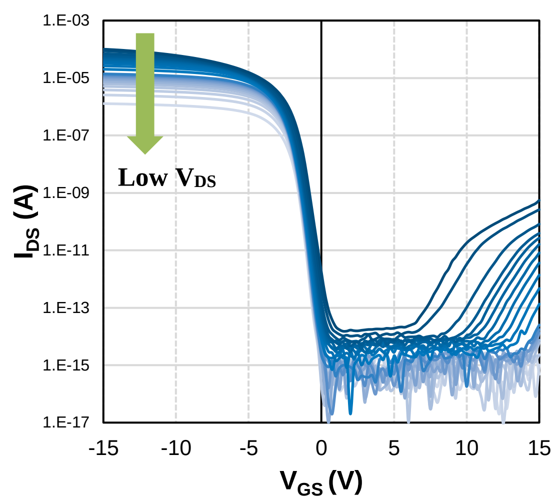

Figure 4. Transfer Curves for LTPS TFTs according to V_{DS} change. V_{DS} range for the measurement is -0.1V to -10.1V.

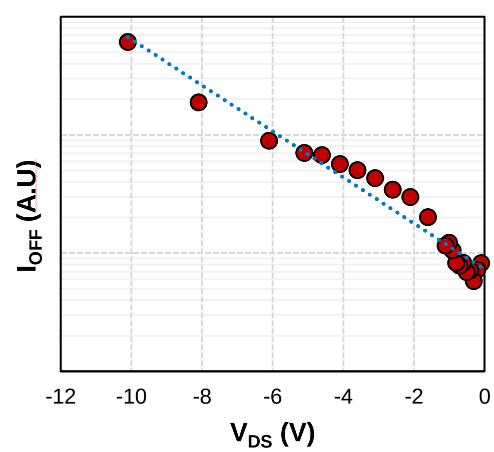

Figure 5. Off leakages according to V_{DS} change with LTPS TFTs. V_{DS} range for the measurement is -0.1V to -10.1V.

An additional hypothesis that can be discussed, which is the real leakage level is located lower than the experimental values by measurement. This is because current data can be viewed as noise level in the low V_{GS} vicinity than the high V_{GS} (>10V), where the GIDL tail is appeared. When considering the relationship between the space charge and the surface potential, the space charge exponentially drop to a discontinuous minimum value through the sequence of accumulation to depletion, weak inversion, and strong inversion. Therefore, the V_{GS} area (0-5V) with the minimum off current in the Figure 2 (b) is considered to be the noise of the measurement system, which means the real off current would be located under the noise current in range of sub-femto amperes. For more accurate off current measurement, a measurement system for atto-ampere is required.

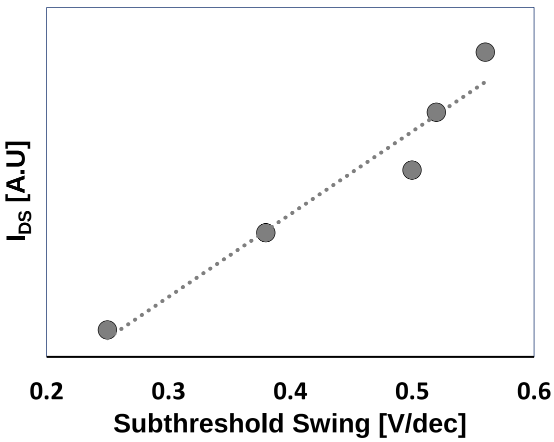

Figure 6. Reduction of off leakage current according to subthreshold swing of LTPS TFTs

Table 1. TFTs data with different process conditions

	I_{OFF}[%]	S.S.	DIBL
Condition	100.0	0.56	0.60
Recipe1	80.3	0.52	0.48
Recipe2	61.3	0.50	0.41
Recipe3	40.8	0.38	0.26
Recipe4	8.8	0.25	0.14

5. Conclusion

In the mass production method in SDC, femto ampere level OFF leakage current was confirmed in LTPS TFTs with the aging process. It was found that the poly-Si TFTs crystallized by the ELA method can have lower leakage than c-Si TFTs. Also, the correlation between V_{DS} and off leakage was confirmed and will be helpful to select off-driving voltages. Finally, this work is expected to be applied further improve image quality and to be able to play an important role in implementing the low-frequency operation for low power consumption.

6. Reference

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