Interfacial Oxidation Layer for Reliable Vertical Thin-Film Transistors

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Abstract

A new fabrication method for vertical thin-film transistors has been developed, where traditional spacers are replaced with gate metals and interlayer dielectrics are substituted with interfacial oxide layers. This approach simplifies the manufacturing process while forming distinct interfacial oxide layers at the upper and lower regions of the vertical thin-film transistor structure. Previous experimental results indicated a significant difference in breakdown voltage between the upper and lower interfacial oxide layers, with the lower layer demonstrating superior electrical performance under applied voltage. For a more thorough analysis, three different structures were analyzed to evaluate the detailed characteristics of the interfacial oxide layers. The analysis included variations in annealing temperature and time. Additionally, the overlap region between the Indium Tin Oxide and gate metal was examined to identify the thickness distribution. A comprehensive evaluation was conducted, encompassing thickness measurements, structural analysis, breakdown voltage assessments, and compositional analysis. The experimental results demonstrated an optimal interfacial oxide thickness, stable breakdown voltage, and favorable compositional properties, making it well-suited for low-voltage operation. These findings validate the potential of interfacial oxidation as an effective gate insulator, paving the way for simplified, scalable, and cost-effective vertical thin-film transistor fabrication processes for next-generation electronic devices.

Author Keywords

Vertical Structure TFTs; Interfacial Oxidation; Gate Insulator Optimization; Low-Voltage Operation.

1. Introduction

The growing demand for high-performance and high-density displays has exposed the limitations of traditional planar Thin-Film Transistors (TFTs) based on two-dimensional (2D) device structures. These limitations include scalability challenges and increased process complexity, which hinder their application in next-generation electronic devices. To address these challenges, researchers have explored innovative three-dimensional (3D) device architectures [1]. Among these, Vertical Thin-Film Transistors (VTFTs) have emerged as a promising solution, offering significant advantages such as minimized device footprints, enhanced spatial efficiency, and reduced power consumption [2]. By defining channel lengths through spacer thickness rather than traditional lithography, VTFTs eliminate the need for advanced lithography equipment, enabling the development of high-resolution and energy-efficient electronic devices [3]. Despite these advantages, VTFT fabrication faces challenges in simplifying the manufacturing process while maintaining reliable electrical and structural performance. Traditional fabrication methods often involve complex, multi-step procedures, such as spacer layer deposition and interlayer dielectric (ILD) integration, which lead to increased process time, cost, and reduced scalability [4]. To address these limitations, our previous work introduced a novel VTFT fabrication method that replaces traditional spacers with gate metals and utilizes thermal annealing to form interfacial oxide layers as substitutes for ILD [5]. This approach leverages the natural oxidation reaction between Tantalum and Indium Tin Oxide (ITO), facilitated by Tantalum's low Gibbs free energy, to simplify the gate insulator fabrication process while enhancing device reliability. Building upon this foundation, the current study focuses on optimizing the interfacial oxide layers to further enhance VTFT performance. Comprehensive analyses were conducted to evaluate the structural and electrical properties of these layers, including thickness, composition, breakdown voltage, and morphology. By identifying the optimal conditions for interfacial oxidation, this research aims to establish a robust, scalable, and cost-effective manufacturing process for VTFTs, paving the way for next-generation electronic devices that meet the demands for high resolution, low power consumption, and scalability.

2. Experiments

The fabrication process of VTFTs began with sequential substrate cleaning using acetone, IPA, DI water rinses, and N_2 rinses to ensure the removal of contaminants. Commercial ITO glass substrates with pre-deposited polycrystalline ITO (Poly-ITO) layers were used. The Poly-ITO layer was patterned using a photomask to define the source electrode structure. Subsequently, a negative photoresist was applied to create a lift-off pattern for the next deposition steps. Tantalum and Indium Tin Oxide (ITO) were chosen as the gate and drain materials, respectively. These materials were deposited sequentially using DC sputtering for Tantalum and DC Pulse sputtering for ITO. Tantalum was sputtered to thicknesses of 200 nm, 300 nm, 400 nm, and 500 nm, while ITO was deposited with a consistent thickness of 100 nm. After the sequential deposition, the lift-off process was performed to create vertical sidewall structures characteristic of VTFTs. To form interfacial oxidation layers between the metal electrodes and the oxide layer (ITO), thermal annealing was conducted in a furnace under various temperatures and durations. This process aimed to investigate the formation and characteristics of interfacial oxide layers at different positions within the structure. Multiple samples were prepared and analyzed to evaluate the structural and electrical properties of the interfacial oxide layers, providing insights into the impact of annealing conditions on the performance and reliability of VTFTs.

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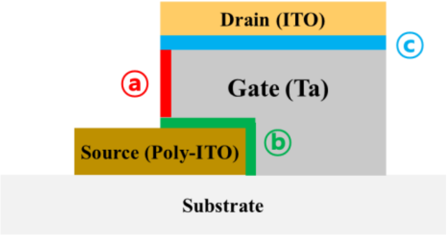

Figure 1. Interfacial oxide layers formed at three distinct regions of the VTFT structure after thermal annealing: upper, lower, and exposed metal regions.

Three junction structures related to VTFTs utilizing an interfacial oxide layer as the gate insulator were fabricated, as shown in Figure 1. These structures were designed to investigate the characteristics of the ⓐ, ⓑ, and ⓒ interfaces within the VTFT structure. The design and fabrication of these structures were based on prior studies to systematically analyze the impact of interfacial oxide formation on the electrical and structural performance of VTFTs.

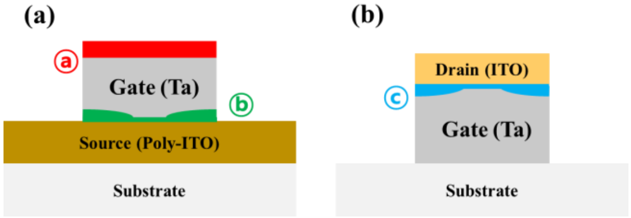

Figure 2. Structures for testing interfacial oxide layer changes due to oxygen diffusion.

The fabricated VTFT structures consist of three distinct regions: two regions where metal electrodes are interfaced with the oxide layer and one region where the metal electrode is exposed to the external environment. To analyze the changes in the interfacial oxide layer due to oxygen diffusion during thermal annealing, additional experiments were conducted. As shown in Figure 2, the ⓑ interface, where the metal is deposited on the oxide layer, and the ⓐ interface, where the metal is exposed to the external environment, were analyzed using the structure depicted in Figure 2(a). Similarly, the ⓒ interface, where the oxide layer is deposited on the metal electrode, was investigated using the structure depicted in Figure 2(b). These analyses provided critical insights into the formation and characteristics of interfacial oxide layers at different locations within the VTFT structure, contributing to a deeper understanding of the effects of thermal annealing conditions on interfacial properties and device performance.

3. Result and Discussion

Tantalum (Ta) was selected as the gate metal for VTFT fabrication due to its low Gibbs free energy (−1911.2 kJ/mol), which promotes efficient oxidation and the formation of stable interfacial oxide layers [6]. The fabricated VTFT structures exhibited distinct interfacial oxide layers at the upper and lower regions, each demonstrating unique electrical and structural properties. To confirm the formation of these oxide layers, FIB-SEM analysis was conducted, revealing consistent growth of the oxide layers at the metal-oxide interface. The thickness of the interfacial oxide layers increased uniformly with rising annealing temperatures of 350 °C, 400 °C, and 450 °C.

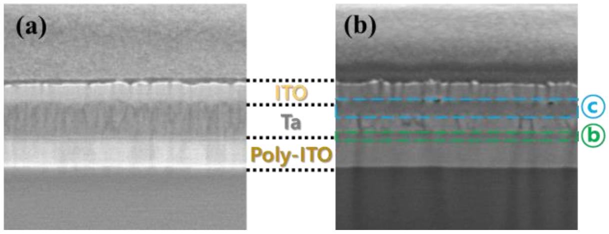

Figure 3. FIB-SEM images of oxide layers formed at each interface after thermal annealing.

Breakdown Field Strength (BFS) measurements under these annealing conditions showed that the lower interfacial oxide layer exhibited superior electrical stability compared to the upper layer, as shown in Figure 3.

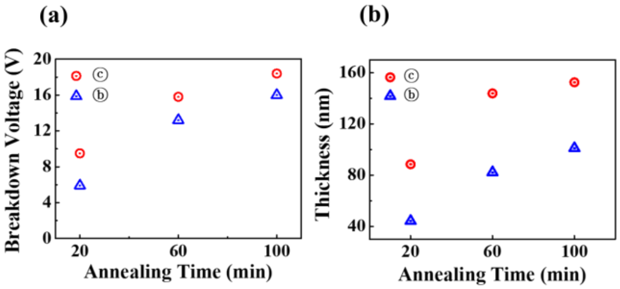

Figure 4. (a) Breakdown voltage of interfacial oxide layers at each position as a function of annealing time, and (b) thickness of interfacial oxide layers as a function of annealing time.

This difference was attributed to variations in oxidation conditions and material interactions at each position. Among the tested conditions, 450 °C yielded the most favorable results, achieving an optimal balance between oxide thickness and process stability. At this temperature, the interfacial oxide layers exhibited enhanced uniformity and electrical performance, making 450 °C the optimal annealing temperature for VTFT fabrication.

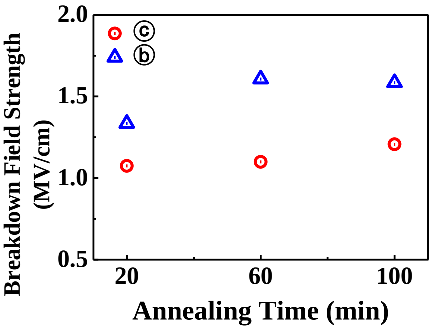

Figure 5. Breakdown Field Strength graph calculated based on breakdown voltage and oxide layer thickness.

Subsequently, the time-dependent effects of annealing at 450 °C were analyzed with durations of 20 minutes, 60 minutes, and 100 minutes. Results indicated that a duration of 60 minutes provided consistent and reproducible interfacial oxide layer properties, while longer durations offered minimal additional benefits in terms of breakdown voltage. Thickness measurements under these optimized conditions revealed that the oxide layer at the edges of the Indium Tin Oxide (ITO) region was thicker than in the inner regions. This observation suggests enhanced oxygen diffusion and interactions at the ITO edges, leading to more pronounced oxidation.

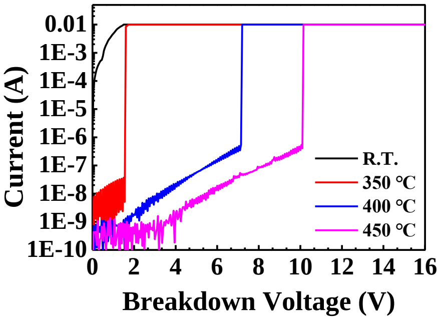

Figure 6. Breakdown voltage graph of surface oxide layers as a function of annealing temperature.

The combination of Tantalum's low Gibbs free energy, optimized annealing parameters, and robust interfacial oxide properties validates the effectiveness of using interfacial oxidation as a gate insulator in VTFTs. These findings demonstrate the potential to replace traditional spacers and interlayer dielectrics (ILD) with interfacial oxide layers in VTFT fabrication, offering a simplified and scalable manufacturing process. The superior electrical stability and structural properties of Ta-based interfacial oxide layers provide valuable insights into advancing VTFT technology for next-generation electronic devices.

4. Conclusion

This study demonstrates the feasibility of utilizing interfacial oxidation as a gate insulator in vertical thin-film transistors (VTFTs), replacing traditional spacer and interlayer dielectric (ILD) layers. Tantalum (Ta) was selected as the gate metal due to its low Gibbs free energy, enabling efficient and stable oxide formation. Experimental results revealed distinct characteristics of interfacial oxide layers at the upper and lower regions of the VTFT structure, with the lower oxide layer exhibiting superior electrical stability due to its enhanced uniformity and material interactions. By optimizing thermal annealing conditions 350 °C, 400 °C, and 450 °C for durations of 20, 60, and 100 minutes it was determined that 450 °C and 60 minutes provided the most reliable and consistent interfacial oxide layers. In contrast, lower temperatures (e.g., 350 °C) resulted in insufficient oxide growth, and longer annealing durations (e.g., 100 minutes) offered minimal additional improvements. Thickness analysis revealed that the oxide layer at the edges of the Indium Tin Oxide (ITO) region was thicker than in the inner regions, attributed to enhanced oxygen diffusion and interaction at the edges. Breakdown voltage tests further validated the robustness of the oxide layers, confirming their suitability for low-voltage applications. These findings highlight the potential of interfacial oxidation to replace traditional VTFT fabrication methods, simplifying processes while ensuring scalability and cost-effectiveness. This approach directly addresses the demands for high resolution, low power consumption, and enhanced reliability in next-generation electronic devices, providing a foundation for advanced manufacturing solutions.

5. References

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