

Insight into the Effect of the Thickness of Gate Insulator on the Hysteresis by TCAD Simulation

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Abstract

The effect of thickness of gate insulator (GI) film on the performance of hysteresis has been investigated by numerical simulation. With the thickness of GI increasing, the hysteresis become worse. The proportion of surface charge potential on surface potential determined the sensitivity of threshold voltage shift. The thick GI brings the high proportion of surface charge potential, triggering the large threshold voltage shift and then leading to the deterioration of hysteresis. We believe that the hysteresis is greatly influenced by surface charge potential. Rationally designed simulation mode will help us interpret the phenomenon of experiment results comprehensively.

Keywords

Gate insulator, hysteresis, thickness, surface potential, surface charge.

1. Introduction

With the increasing demand for flexible displays, organic light-emitting diode display technology has undergone rapid and robust development [1]. The low temperature polysilicon thin film transistor (TFT) is used to drive each pixel for its high electron mobility and current driving capability, stable current-voltage characterization [2, 3]. Due to the need for high-quality display of customers, the requirement of TFT is also increasing. There still are some drawbacks in TFT need to be solved [4-6]. Wherein, hysteresis would cause image sticking (IS) and other display issues [7]. Hysteresis is highly undesirable in logic devices, sensors, and driver devices, as it can cause a shift in threshold voltage when the voltage scanning direction or range changes, especially near subthreshold states [8]. There is consensus over several of the factors that would cause hysteresis, including trap states in the dielectric, on the dielectric surface or at semiconductor/dielectric interface, fixed charges in the dielectric and etc [9-11]. Many researchers all the world denote lots of efforts to relief this problem, such as: clean & passivated silicon surfaces, choicing better material of suitable gate insulator, improving the thermal process to eliminate interface defects, etc [12-14]. However, there are still some issues about hysteresis need to be solved. Especially, the thickness of gate insulator (GI) film would influence the hysteresis, but the mechanism isn't clarity [13].

In this work, we study the thickness of GI induced the shift of hysteresis by establishing the physical model via Silvaco TCAD. The increased thickness of GI would give rise to the deteriorated hysteresis, which is mainly contributed by the ionization of interface trap state and influence of interface potential on threshold voltage (V_{th}). It is found that the influence of interface potential on V_{th} makes a decisive input and the high proportion of surface charge potential significantly improve the shift of ΔV_{th} ($\Delta V_{th} = V_{th-reverse} - V_{th-forward}$) and worse hysteresis for thick GI. The final simulation results are well consistent with the experiment results, confirming the high accuracy of numerical simulation. And we conducted experiments to validate this conclusion by manufacturing OLED panels with thinner gate

insulator layers, confirming that this is highly beneficial for improving the IS.

2. Experiment

A low temperature polycrystalline silicon TFTs were integrated on a glass substrate. The polysilicon has a channel width to length ratio (W/L) of 3.3 $\mu\text{m}/18 \mu\text{m}$ with the polysilicon thickness of 45 nm. SiO_2 (120 nm or 180 nm) was used as gate insulator and was deposited by the plasma-enhanced chemical vapor deposition (PECVD). Metal was deposited using plasma-enhanced physical vapor deposition (PEPVD) and patterned by dry etching, Mo is used to form the gate electrode, while Ti is utilized for the source and drain electrodes. The TFT transfer characteristic curves were measured at room temperature by semiconductor parameter analyzer Keithley 4200.

3. Results and Discussion

The electronic properties of TFT with different GI thickness were characterized, and the V_{th} value has been extracted from measured curve. As shown in Figure 1, during the enhancement of GI from 120 nm to 180 nm, the hysteresis degradation worsens. It indicates that the deterioration of hysteresis occurs. However, it is difficult to clarify the mechanism of GI thickness effect on hysteresis solely through experiment.

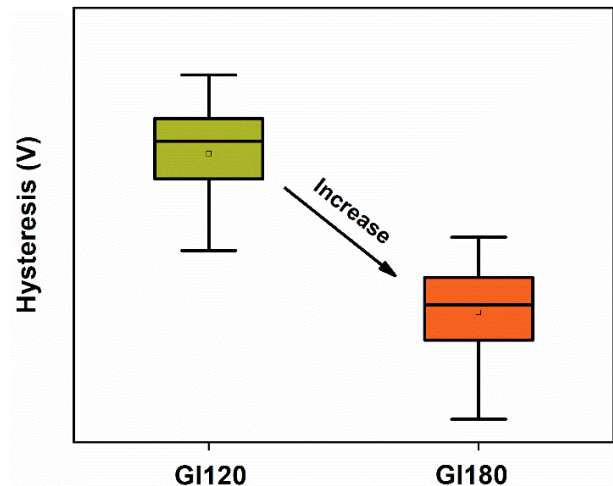


Figure 1. The threshold voltage shifts of TFTs with different GI thickness.

In order to solve above issue, we established a simulation mode based on the Heiman model [15]. The TFTs with different thickness of GI have been created, which are denoted as GI120 and GI180, and the interface in GI layer obtains native trap states in several nanometers which is the mainly composition of surface charge potential. Under the excitation of an electric field, the trap states near the interface gradually undergo ionization from shallow to deep, and as the voltage increases, deeper trap states undergo ionization, finally, leading to the change of transfer characteristic curve in the forward and reverse scanning [16].

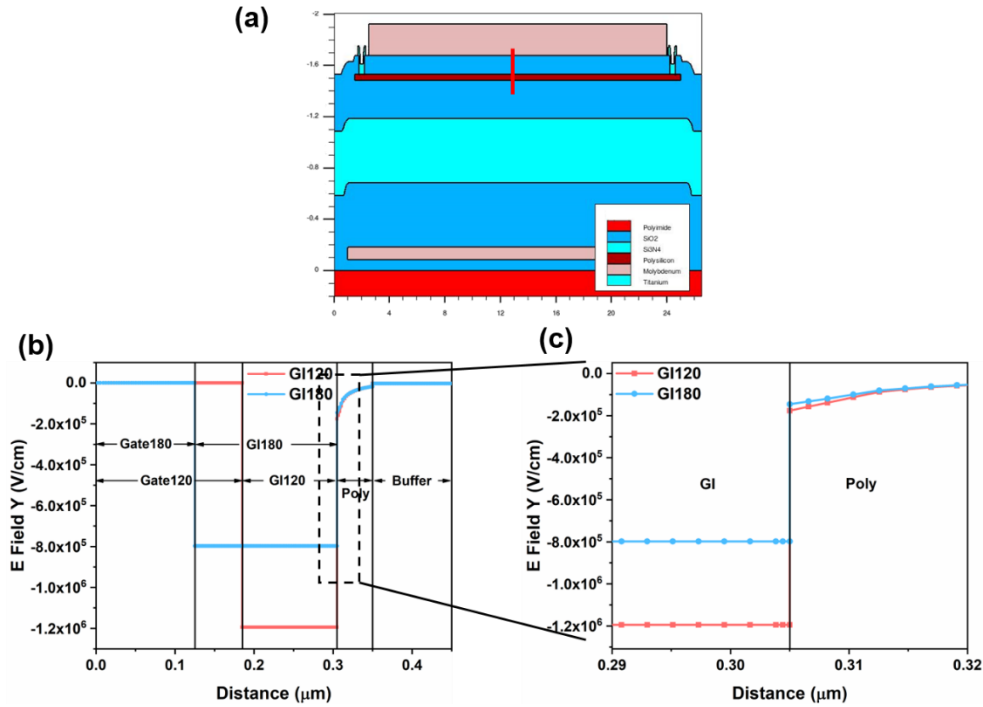


Figure 2. (a) Schematic of TFT and the value position (red line); (b) (c) The electric field distribution of TFT with different thickness of GI.

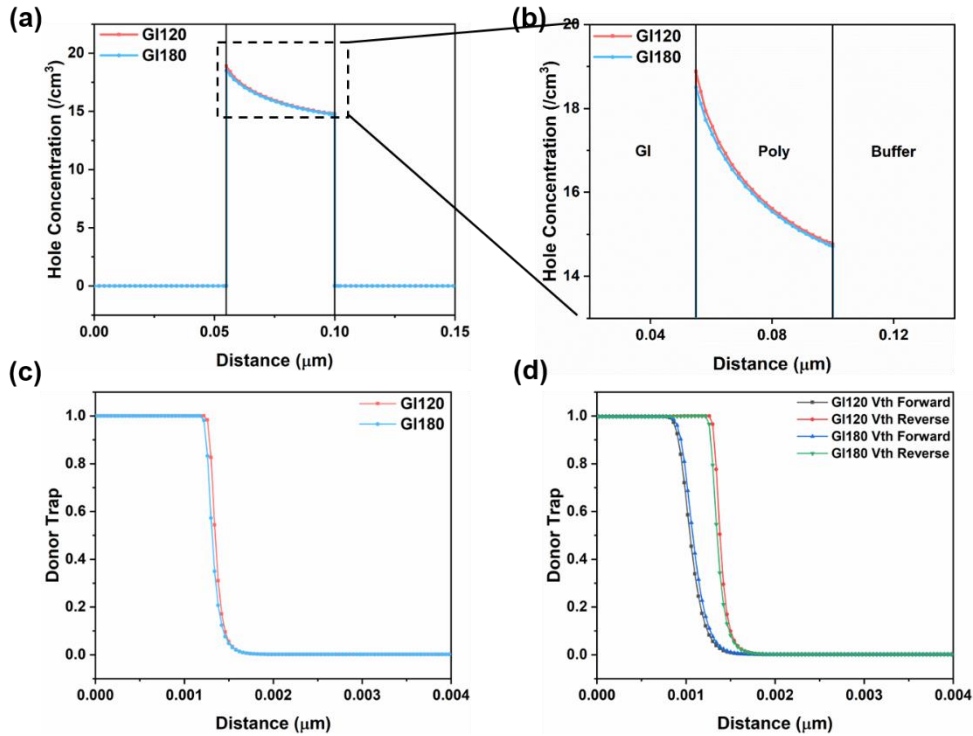


Figure 3. (a) (b) The hole concentration distribution with different thickness of GI; (c) the ionization degree of surface trap under -15 V; (d) the ionization degree of surface trap when scanning is forward and backward to V_{th} .

As the thickness of GI increasing from 120 nm to 180 nm, the partial voltage of GI increases due to the higher resistance of 180 nm sample, causing the relatively lower partial voltage on the

polysilicon which are shown in Figure 2a-c. The weak electric field of polysilicon reduces the migration of charge carriers in semiconductors, leading to a decrease in the number of charge

carriers in the channel (Figure 3a, b). According to the Heiman model, the time constant τ of a trap is the mean time before the trap captures a carrier. It depends on the concentration of carriers available for trapping, and is independent of the number of trap. Back to our mode, under the same bias, the less charge carriers in channel would diminish the capture cross section of trap and reduce the capture process. Therefore, in order to verify this assumption, the degree of ionization of trap states have been simulated with the gate voltage at -15 V, which is illustrated in Figure 3c. It can be obtained that the thicker GI would decrease the ionization depth of trap state, even though this change is slight.

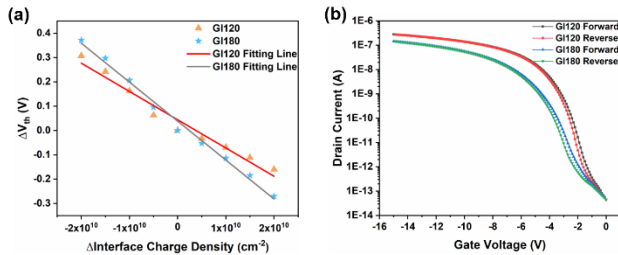


Figure 4. (a) The variation of ΔV_{th} on the change of surface charge; (b) the transfer characteristic curve of TFTs with different GI thickness by simulation.

The apparent phenomenon of hysteresis is the difference in V_{th} between the forward and backward scanning processes. The ionization depth curve of trap states under characteristic voltage (V_{th} of each TFT, obtained forward and backward) is calculated. As shown in Figure 3d, in forward scanning process, the gate voltage scans from 0 V to each V_{th} . In the initial state, these two TFTs keep off and at final state (at each V_{th}), the thick GI brings negative shift of V_{th} , which induced heavy ionization of trap states. In the backward scanning process, the gate voltage scans from -15 V to each V_{th} . At the gate voltage of -15 V, the thicker GI acquires the shallower ionization depth. During the backward scanning, with the gate voltage gradually increasing which is still under the negative range, this process is accompanied with the deionization and ionization. At the V_{th} point, the degree of ionization of trap states will be severely affected by the initial state at -15 V. The GI180 sample will always maintain the lower ionization degree, which is only 83.2% of thinner one. From this result, GI180 has slight change of ionization of Heiman trap state in forward and reverse scanning. Nevertheless, the less ionization will trigger the less hysteresis, which is inconsistency with the measured result.

The above result indicates that there is still a more significant factor that hasn't been considered. Extract from experiment results that the small change in interface charge (the thicker GI) could have a significant impact on the variation of V_{th} value. A reliable assumption has been proposed that the sensitivity of ΔV_{th} to interface charge change has discrepancy as the thickness of GI altering. By adjusting the interface charge density in our mode, the ΔV_{th} has been discussed. In the Figure 4a, it apparently shows that the ΔV_{th} of thicker GI sample is more sensitive in the change of interface charge. The rate of change of the two samples (-1.60×10^{-11} V/ cm^{-2} and -1.16×10^{-11} V/ cm^{-2} for GI180 and GI120, respectively) was quantified by linear fitting. The sensitivity has enhanced about 38.03%, which maintain the same tendency of measured results. We can speculate that the sensitivity of charge change plays a crucial role in the variation of V_{th} . We define the total influence co-efficient as the ratio of

ΔV_{th} between two samples. The experimental influence coefficient is 1.20. For the simulation result, taking the previous factor into account, simulative influence co-efficient can be obtained by overlap these two factors (ionization degree and interface potential), and simulative influence co-efficient is 1.15, which is the product of 1.3803 and 83.2%. The similar result of experiments and simulations indicates that the simulation results have high feasibility (Figure 4b).

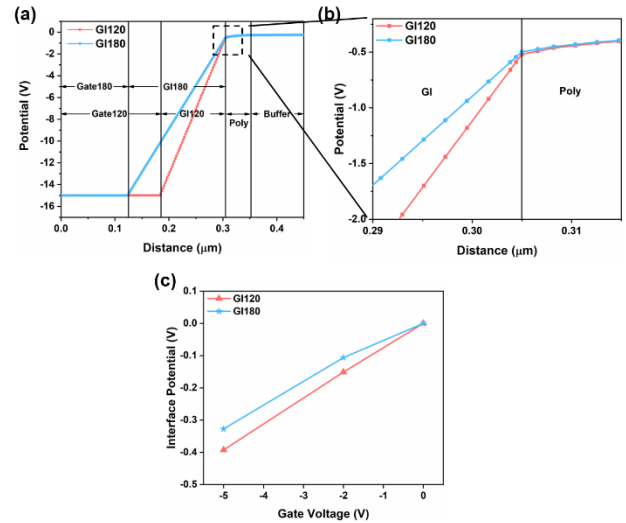


Figure 5. (a) (b) The distribution of potential on TFT with different thickness of GI; (c) surface potential of polysilicon under different gate voltage.

In this system, the surface potential is composed by the gate voltage and surface charge potential that is stemmed from interface trap state [17, 18]. According to above discussion, the thickness of GI has little effect on the density of interface trap states. Hence, we can assume that the surface charge density of TFT with different thickness of GI is approximately equal. In addition, the thicker GI would increase the loading amount of gate voltage on GI, and the corresponding decrease of loading amount of gate voltage will take place on polysilicon surface, finally, attributing to decrease the control ability of gate voltage on the surface potential of polysilicon (Figure 5). The contribution of interface charges to surface potential increases, causing the amplified ability of surface charges to control the surface potential. A high proportion of surface charge potential can significantly affect the variation of V_{th} under the same surface charges change. Therefore, GI180 sample represents the large ΔV_{th} and deteriorated hysteresis. This phenomenon suggests that the interface potential is the key factor on the hysteresis issue of TFTs.

4. Conclusion

In summary, we have elucidated the impact of GI thickness on hysteresis by numerical simulation. The thicker GI would cause the severe hysteresis. Meanwhile, the ionization of surface states and the composition of surface potential will be both affected by the thickness of GI. However, surface charge potential dominates the change of V_{th} due to the different proportion of surface charge potential on surface potential. With the increasing thickness of GI, the proportion of surface charge potential increases, causing the high sensitivity of ΔV_{th} on surface potential and worse hysteresis. Furthermore, rational design of numerical simulation structure can help us understand and explicate the phenomenon

encountered in experiments.

5. References

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