An Advanced Flexible OLED Anti-ESD Design

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Abstract

As OLED screens gain increasing recognition in the market, they have become the standard for mainstream high-end products. However, the OLED process is complex, involving numerous steps, and is prone to ESD issues, which negatively impact product yield and pose challenges to OLED production. To improve the anti-ESD ability of the screen process, the mechanism of ESD occurrence is analyzed, and product design is optimized to enhance the anti-ESD ability. Three main approaches are implemented: first, adjusting the ESD circuit design to optimize the electrostatic discharge channel; second, optimizing the structure design of TFT devices to improve their anti-ESD capability; and third, applying an organic film layer to the screen to block electrostatic intrusion. These optimizations successfully reduce the ESD incidence rate from 7.5% to 0.1%.

Keywords: OLED; ESD; Anti-ESD

1. Introduction

Designers have implemented various measures to protect OLED screens from ESD. One commonly used method is the application of TVS diodes for ESD protection. Typically, TVS diodes are connected in parallel to key signal lines, leveraging their fast response and stable clamping capabilities to dissipate accumulated high voltage in a short time, thereby protecting the circuit board. The layout of internal components in screen design is also critical. For electrostatically sensitive components, such as MOS SFRT and CMOS integrated circuits, it is essential to position them away from areas prone to static electricity. In addition, signal lines should be kept as short as possible, as longer lines are more susceptible to static induction. At the same time, ground wires can be added during wiring to discharge static electricity and direct it to the ground. For high-speed signal lines, more attention should be paid to the spacing of the remaining surrounding lines to prevent electrostatic coupling interference. Beyond circuit design improvements, a GuardRing can also be designed on the mask to prevent static electricity.

To improve the ESD resistance of the screen process, we have analyzed the mechanism of ESD occurrence and optimized product design. Three main solutions are implemented. First, adjusting the ESD circuit design by replacing the double-tube design with a single-tube design, modifying the ESD circuit *W/L* ratio, and increasing the data routing capacitor to optimize the electrostatic discharge channel. Additionally, the pad is shorted to the mask GuardRing to balance static accumulation on the exposed pad. Second, the structural design of TFT devices is optimized by increasing the distance between CNT and Gate to enhance the device's ESD resistance. Third, an organic film layer is applied to the screen to block static electricity from penetrating the screen. Through these design optimizations, the process ESD incidence rate has dropped from 7.5% to 0.1%.

This paper focuses on how to optimize panel design to improve ESD resistance by adjusting the ESD circuit design and optimizing the structural design of TFT devices.

2. Adjusting the ESD circuit design

The main purpose of the ESD circuit is to reduce voltage and current, thereby protecting other circuits. With the development of panels toward higher frequencies, faster speeds, and greater integration, ESD protection circuit design faces new challenges. Therefore, adjusting the ESD circuit design and optimizing the electrostatic discharge channel are crucial for improving the anti-ESD ability of OLED screens.

There are two main aspects to adjusting the ESD circuit design. The first is to use ESD single tube design. When the circuit is working normally, the ESD circuit is in the cut-off state. When the voltage reaches the breakdown threshold, the circuit quickly transitions to a low-resistance state, providing a conduction path for instantaneous current and protecting other circuits. As shown in Figure 1, the double-tube ESD design has a higher breakdown voltage. However, for the protection of other circuits, the presence of only a single TFT in the ESD circuit facilitates easier discharge of ESD. In comparison, the switch to a single-tube ESD design offers better protection for other circuits.

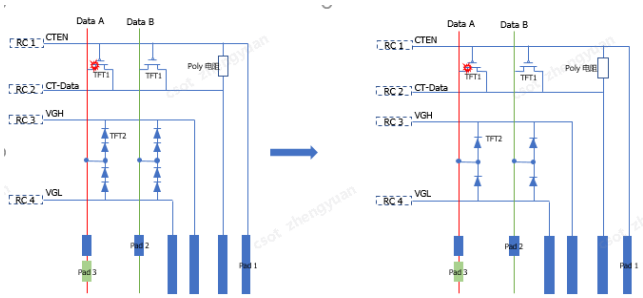

Figure 1. The mechanism diagram of ESD circuit blast.

The second is to use mask electrostatic rings, as shown in Figure 2. The closed GuardRing formed by metal layers on the mask connects dummy patterns. However, this design can only protect the peripheral ESD, no ESD protection effect within the panel. In order to improve this problem, the panel pad is extended out of the panel through poly layer lead wires and connected to the peripheral GuardRing. This design is aimed at balancing the accumulation of electrostatic discharge during the manufacturing process to prevent electrostatic discharge injury (ESD injury) that may arise from excessive static electricity in a single routing line.

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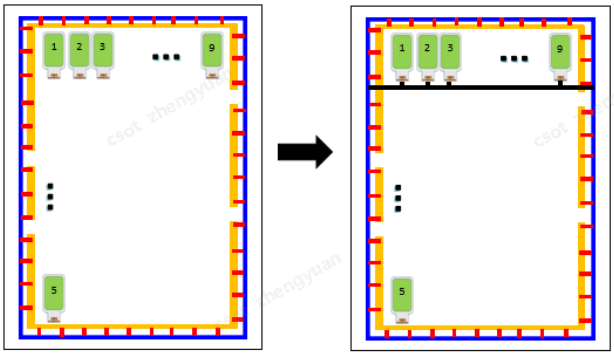

Figure 2. The mask electrostatic rings for ESD protection.

3. Optimizing the structural design of TFT devices

Another solution is to optimize the structural design of TFT devices to enhance their anti-ESD capability. As shown in Table 1, we verify the anti-ESD ability under different schemes. Increasing the distance between CNT and GE1 is an effective way to improve the device's ESD resistance. By increasing this distance, the electric field strength between the gate and the source/drain during ESD events is reduced. Since the electric field strength is inversely proportional to the distance, when the distance increases, even if there is a certain amount of charge accumulation, the generated electric field strength will be relatively reduced, thereby reducing the risk of breaking through the insulation layer and forming a current channel to cause device failure. Widening the width of VGH/VGL increases the capacitance between the traces and surrounding structures. This increased capacitance can play a certain buffering role in ESD events, helping to absorb and disperse the energy of ESD pulses. This reduces the peak current of ESD pulses, thereby minimizing damage to sensitive circuit components and improving overall circuit protection. Additionally, widening the width of the ESD protection circuit can reduce the resistance of the trace, providing a wider current discharge channel during ESD events. This allows ESD current to be directed to the ground or other safe paths more quickly and smoothly, reducing current accumulation within the device and lowering the risk of device damage due to excessive current.

Tabel 1 ESD resistance under different verification conditions

Case	Detail	Anti-ESD ability
1	CT circuit CNT to GE1 space compression	Reduced
2	CT circuit CNT to GE1 space increase	Improved
3	Adjusting the *W/L* value of the ESD circuit	Improved
4	Widening the VGH/VGL width of the ESD circuit	Improved

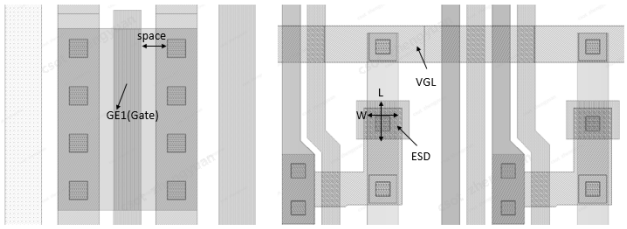

Figure 3. The ESD device circuit diagram.

4. Conclusion

In this work, we propose three solutions to improve the anti-ESD of the screen process. First, the ESD circuit design is optimized by adopting a single-tube design, adjusting the *W/L* ratio, and increasing the data routing capacitor,Furthermore, we balance the accumulation of static electricity on the exposed pad by short-circuiting it to the Mask Guard ring. Second, the structural design of TFT devices is improved by increasing the distance between CNT and Gate and widening the width of VGH/VGL traces. Third, an organic film layer is applied to the screen to block static electricity generated during the EL process from penetrating the screen. These optimizations successfully reduce the ESD incidence rate from 7.5% to 0.1%.

5. References

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