Improved PBTS Reliability of Dual-Gate a-IGZO TFT by Bottom Interface Optimization

Hanpeng Deng*, Yuanpeng Chen*, Xingyu Zhou*, Wei Wang*, Yanqing Guan*, Chao Dai*, Ming-Chou Wu*

*** Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd., Wuhan, China**

Abstract

Amorphous transparent oxide TFT based on a-IGZO has been widely used in OLED display fields. In practical applications, we find that compared with the single top gate structure, the dual-gate a-IGZO TFT has higher current to meet strict display requirements, but the reliability will deteriorate to limit its further development. Firstly, we confirm that under PBTS test, the bottom channel interface of dual-gate IGZO TFT exhibits significantly larger Vth shifts than the top channel interface (top and bottom channel contributions are 0.11V and 0.63V, respectively). The worse reliability is mainly due to the damage to the interface caused by ion bombardment during a-IGZO deposition, which inevitably generates a large amount of unbonded or free oxygen at the interface. These defects trap carriers accumulating negative charges at the interface, thereby shielding part of the gate electric field and causing Vth shift. Therefore, we propose that by increasing the hydrogen content in the bottom gate insulation layer, more hydrogen diffused to the interface can passivate the excess oxygen defect. The significant improvement results show that the Vth shift of dual-gate IGZO TFT under PBTS decreases from 0.81V to 0.41V.

Author Keywords

a-IGZO TFT, PBTS Reliability, Interface Optimization, Oxygen Defect.

1. Introduction

Hideo Hosono first proposed a new semiconductor material, transparent amorphous oxide semiconductor from In-Ga-Zn-O system (a-IGZO), for the active channel of transparent thin film transistors (TFT) [1]. After over 20 years of development, dual-gate a-IGZO TFT with both top-gate and bottom-gate drives have been widely used in organic light-emitting diode (OLED) display backplane technology, such as mobile phones, tablets, watches and so on. The dual-gate a-IGZO TFT can meet the current required for high frequency display, as well as low leakage current and low power consumption. Despite the many advantages, its reliability in applications still faces some challenges.

In practical applications, we find that the dual-gate a-IGZO TFT always exhibits worse reliability than top-gate TFT (which still has a bottom metal layer connected to the source, acting as a light shielding layer). This is manifested as a larger threshold voltage (V_{th}) shift after a long period of operation. Therefore, in this study, we adopted Positive Bias Temperature Stress (PBTS) to accelerate the simulation of TFT long-term operation. By comparing the characteristics changes of dual-gate a-IGZO TFT under top gate and bottom gate PBTS, the main reasons for the deterioration of stability are identified. We also propose an improvement strategy to make TFT devices show excellent reliability.

2. Experiment

The structure of prepared dual-gate a-IGZO TFT is shown in Figure 1. First, a buffer layer was deposited on the glass substrate coated with polyimide (PI). A layer of patterned Mo was then used as the bottom gate electrode (BG) and a layer of both SiOx and SiNx as the bottom gate insulation layer (BGI). Then, the a-IGZO layer was formed by physical vapor deposition (PVD) and patterned as the active layer. SiOx and Mo were then deposited to form the top gate insulator (TGI) and top gate electrode (TG). The IGZO pattern in the non-channel area was conducted by ion implantation through the patterned TG. Finally, after interlayer dielectric (ILD) deposited, the source/drain were connected to IGZO through contact holes. The dimensions of the prepared dual-gate a-IGZO TFT are 3 µm wide and 3 µm long.

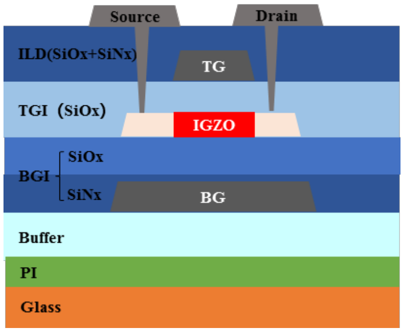

Figure 1. Cross sectional view of Dual-Gate a-IGZO TFT schematic.

The TFT transfer characteristics were measured using an Agilent B1500A semiconductor analyzer during PBTS tests. During the measurement of the I_D–V_G characteristics, the gate voltage was swept from V_{GS} = -10 to +10V while V_{DS}= +0.1/ +5V were applied to the drain terminal (the source terminal was grounded). The TFT threshold voltage was extracted from the I_D–V_G characteristics as the V_G at which the drain current (I_D) equals 10^{-9} A. During PBTS tests, the sample was first heated to 60 °C. The Agilent B1500A then applied the gate stress voltage for duration of 3600s while both the source and drain are grounded (V_S = V_D = 0 V). All stressing and measurements were done in ambient air in the dark. A different device on the same substrate was used for each PBTS test.

3. Results and Discussion

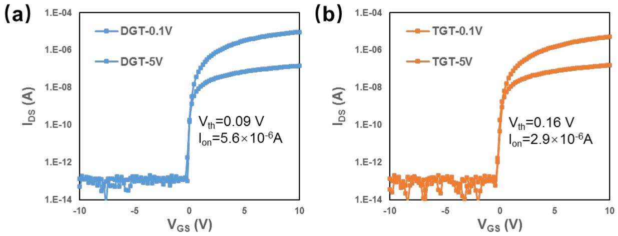

Figure 2. Comparison of initial transfer characteristics of dual-gate device DGT(a) and top-gate device TGT (b).

The prepared a-IGZO TFT has both top and bottom gate metals. It can be used as a top-gate device (TGT) when the bottom gate synchronizes the source signal, and as a dual-gate device (DGT) when the bottom-gate synchronizes the top-gate signal. The

ISSN 0097-996X/25/5603-1498-$1.00 © 2025

comparison of initial characteristics of DGT and TGT is shown in Figure 2. While the difference in V_{th} is small, the drain current of DGT is increased to twice, and the additional current is contributed by the bottom channel. The higher current allows dual-gate devices to meet today's increasing display frequency requirements, but their reliability against positive gate voltages must be studied.

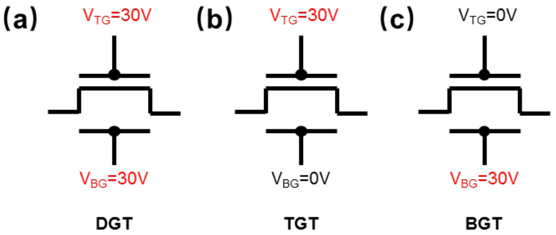

Figure 3. Three different PBTS test methods: Apply positive voltage (a) to the dual-gate, (b) only to the top-gate, and (c) only to the bottom-gate.

The DGT operates with two channels, equivalent to two TFT devices, TGT at the top and BGT at the bottom. According to the test method shown in Figure 3, PBTS were applied to either top-gate or bottom-gate, as well as simultaneously, to analyze the reliability difference between them. Figure 4 shows how the transfer characteristics of the TFT devices for the three test methods change with the PBTS duration, and summarizes their V_{th} shift for direct comparison. Figure 4 (a) shows that DGT exhibits a V_{th} shift of 0.81V after 1h PBTS. By comparison with FIG. 4 (b) and (c), the V_{th} shift of TGT and BGT are 0.11V and 0.63V respectively, and the sum of the two is equivalent to DGT. Therefore, it is easy to conclude that the bottom channel is responsible for most of the deterioration of the reliability of dual-gate a-IGZO TFT.

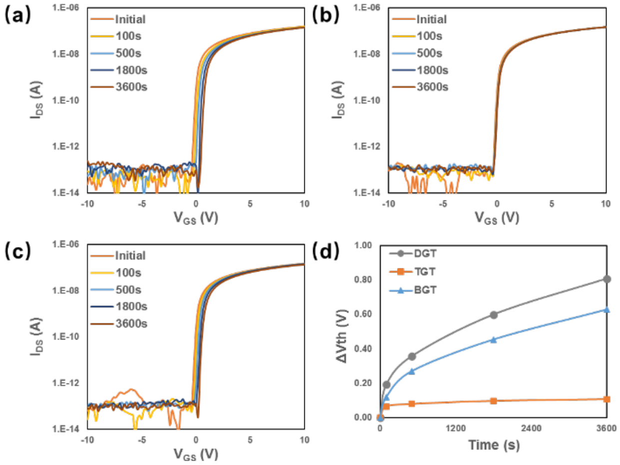

Figure 4. Reliability comparison of three different PBTS voltage stress modes. (a) DGT, (b) TGT, (c) BGT and (d) summary of V_{th} shift.

After decades of development, researchers have reached a basic consensus on the PBTS reliability mechanism of amorphous oxide TFT such as a-IGZO. The phenomenon of a positive threshold voltage shift with an applied positive gate bias results from negative charge being trapped at the channel/dielectric interface or getting injected into the gate dielectric [2]. The positive threshold voltage shift is then explained by the negative charge screening the applied gate voltage. As for DGT with a bottom channel, there are a large amount of defects at the interface between a-IGZO and the BGI layer that can capture negative charges, resulting in poor reliability of PBTS. We speculate that the free oxygen and unbonded oxygen produced by high-energy ion bombardment on the interface in the process of IGZO deposition by PVD are the main components of the defects. The PBTS reliability of TFT at the top is better, mainly because of the difference between PECVD and PVD process, and the treatment of the interface before the TGI layer is formed.

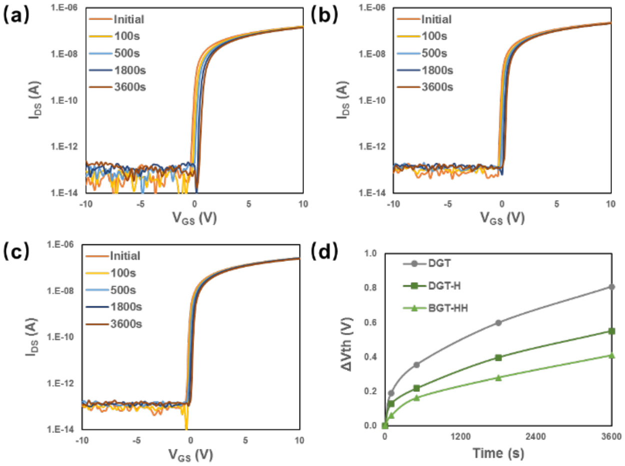

Figure 5. PBTS reliability comparison of devices with different BGI deposition conditions. (a) DGT, (b) DGT-H , (c) DGT-HH and (d) summary of V_{th} shift.

Therefore, the key to improve the PBTS reliability of DGT is to reduce the excess oxygen defects at the bottom interface. We propose that SiOx film with higher hydrogen content can be deposited in the BGI layer by adjusting PECVD process parameters. In the latter high-temperature process, hydrogen diffuses to the interface to combine with oxygen to passivate the defects. Therefore, we prepared two other a-IGZO TFTs with gradually increased hydrogen content of SiOx in BGI, named DGT-H and DGT-HH respectively. Figure 5 shows that the PBTS reliability of the two improved devices is 0.55V and 0.41V, respectively, compared to the reference DGT. The reliability is significantly improved, and it also confirms our speculation about the cause. However, it should be noted that higher hydrogen content will also lead to negative shift in initial V_{th} of the TFT, because some hydrogen uncontrollably diffused into the IGZO to form oxygen vacancies, bringing additional carriers. Therefore, it is necessary to maintain the balance of hydrogen and oxygen at the interface, and the hydrogen content should not be blindly increased, otherwise it will lead to device failure.

4. Conclusion

In conclusion, by comparing the electrical changes of dual-gate a-IGZO TFT from top gate and bottom gate PBTS respectively, focusing on the shift of V_{th}, this paper proves that the deterioration of PBTS reliability is mainly caused by bottom channel. A large number of oxygen defects at the interface between the bottom channel and the bottom gate insulation layer caused by a-IGZO deposition process are the root cause. We propose a strategy of passivating defects by moderately increasing the hydrogen content in silicon oxide in the bottom gate insulation layer by adjusting PECVD process, which significantly improves the reliability of dual-gate a-IGZO TFT. It is hoped that this study can further promote the reliability research of a-IGZO TFT and realize its wider application in display technology.

5. References

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