An AMOLED LTPS Pixel Circuit Compensating for Threshold Voltage Variations, OLED Degradation, and IR Drop

Sanghyun Park[1], Hyunwoo Kim[1], Hojin Lee[1,2*]

[1]Dept. of Intelligent Semiconductor, Soongsil University, Seoul 06978, Korea

[2]School of Electronic Engineering, Soongsil University, Seoul 06978, Korea

Abstract

In this paper, we proposed active-matrix organic light-emitting diode (AMOLED) low temperature poly-crystalline silicon (LTPS) pixel circuit compensating for variations in threshold voltage (V_{TH}), organic light-emitting diode (OLED) degradation, and IR drop. The proposed circuit is composed of six thin film transistors (TFTs) and two capacitors. From the simulation results, the maximum OLED current error rates are 6.76%, 12%, and 5.89%, when the V_{TH} shift is -1 V, the OLED stress time is 40,000 s, and the ELVDD reduction is 10%, respectively.

Author Keywords

Active-matrix organic light-emitting diode (AMOLED); Pixel circuit; Low temperature poly-crystalline silicon (LTPS) thin film transistor (TFT); Threshold voltage (V_{TH}); OLED degradation; IR drop;

1. Introduction

Active-matrix organic light emitting diode (AMOLED) displays have a wide viewing angle, fast response time, wide color gamut, and vivid color, and based on these, they have developed rapidly in recent years. OLEDs emit light by current, and pixel circuits using thin film transistors (TFTs) control the luminance of OLEDs by controlling the amount of current. Low temperature poly-crystalline silicon (LTPS) TFTs have several advantages such as high mobility and electrical stability compared to other TFT technologies. Due to these advantages, LTPS TFTs are widely employed for AMOLED display backplane technology [1], [2], [3]. However, deviation of the threshold voltage (V_{TH}) caused by randomly formed grain boundaries in LTPS TFTs, which negatively affect the driving performance and reliability of AMOLED display [4].

However, AMOLED displays also have to solve other problems, not just variations in the electrical characteristics of TFTs that make up the pixel circuit. The degradation of OLEDs by continuous operation increases the turn-on voltage of OLEDs. The increased turn-on voltage makes it difficult for OLEDs to produce uniform luminance, which is an issue that needs to be addressed to improve the quality of the displays [5], [6].

The voltage reduction of a common voltage source, commonly referred to as the IR Drop, is also an important issue to be addressed. A reduction in the common voltage source, which can occur in the center of the panel, can change the amount of current in the driving transistor [7], [8]. This causes OLEDs that emit light from the center of the panel to emit light with a different luminance than OLEDs that emit light from the edge of the panel. These issues affect the reliability and performance of AMOLED displays, highlighting the importance of developing pixel circuits that can effectively solve external problems as well as driving TFTs of pixel circuits.

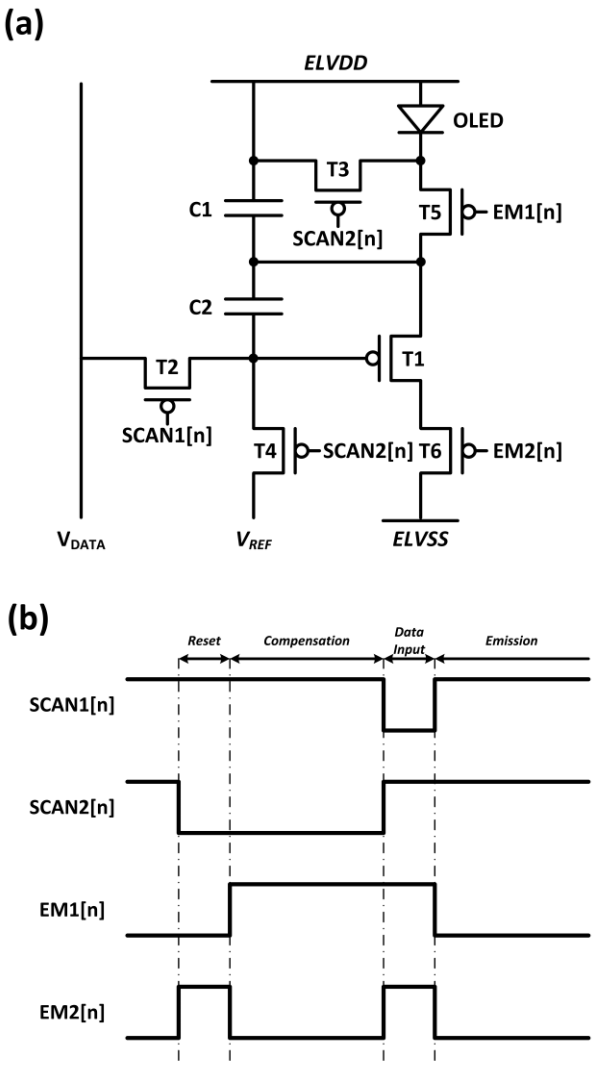

Figure 1. (a) Proposed LTPS pixel circuit schematic and its (b) timing diagram.

In this paper, we propose a novel voltage-programmed AMOLED LTPS pixel circuit compensating for V_{TH} variation caused by randomly formed grain boundaries in LTPS TFTs, OLED degradation resulting from extended stress time, and IR drop. The proposed circuit compensates for the V_{TH} through a source follower mechanism and addresses OLED degradation and IR drop via the coupling effect of the capacitor connected between the source and gate of the driving TFT. The proposed circuit is simulated to drive ultra-high definition (UHD) resolution (3,840 × 2,160) 4K display with a frame refresh rate of 60 Hz.

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2. Proposed Pixel Circuit and Operation

Figure 1. (a) shows the schematic of the proposed 6T2C LTPS pixel circuit. The proposed pixel circuit consists of one driving LTPS transistor (T1), five switching LTPS transistors (T2 to T6), and two capacitors. Figure 1. (b) shows the timing diagram of the proposed pixel circuit. The operation of the proposed circuit is divided into four periods, as described below.

Reset: In the reset period, SCAN2[n] and EM1[n] fall to low voltage, and T3, T4 and T5 are turned on for the initialization. Through T3 and T5, the ELVDD voltage initializes the source node of T1, enabling T1 to operate as a source follower during the compensation period. Also, the reference voltage is applied through T4, initializing the gate node of T1. At this time, since T6 is turned off and the same voltage is applied to both the anode and cathode of the OLED, no current flows through the OLED.

Compensation: In the compensation period, SCAN2[n] maintains low voltage, keeping T3 and T4 on, and EM1[n] rises to high voltage turning off T5. As ELVDD continues to be applied to the cathode of the OLED, the OLED remains stably in the off state. Additionally, a reference voltage is continuously applied to the gate node of T1, and as EM2[n] falls to low voltage, T6 turns on, allowing T1 to operate as a source follower. During this process, the source node voltage of T1 becomes V_{REF} - $V_{TH,T1}$, and the V_{TH} of T1 is stored on C2.

Data input: In the data input period, SCAN1[n] falls to low voltage, and T2 is turned on to apply the data voltage to the gate node T1. At this time, due to the capacitive coupling of C1 and C2, the source node of T1 is as follows:

$$V_{SOURCE,T1} = V_{REF} - V_{TH,T1} + \frac{C2}{C1+C2}(V_{DATA} - V_{REF}) \quad (1)$$

Emission: In the emission period, EM1[n] and EM2[n] fall to low voltage, and T5 and T6 are turned on, forming a current path through T1 and OLED between ELVDD and ELVSS, enabling OLED emission. In this period, the source node of T1 becomes V_{OLED}, and due to capacitive coupling, the gate node of T1 is as follows:

$$V_{GATE,T1} = V_{OLED} + V_{TH,T1} + \frac{C1}{C1+C2}(V_{DATA} - V_{REF}) \quad (2)$$

Therefore, the current flowing through the OLED, determined by T1, is as follows:

$$I_{OLED} = \frac{k}{2}\left(V_{SG} + V_{TH,T1}\right)^2 = \frac{k}{2}\left(\frac{C1}{C1+C2}(V_{REF} - V_{DATA})\right)^2 \quad (3)$$

where $k = \mu C_{OX} W/L$. As shown in (3), T1 operates independently of the V_{TH} and V_{OLED}. Therefore, a constant current can be expected to be maintained despite changes in the electrical properties of the driving TFT or the characteristics of the OLED.

3. Result and Discussion

The proposed pixel circuit is verified with the HSPICE tool from Synopsys. ELVDD, ELVSS and V_{REF} are connected to voltage sources of 5 V, -5 V, and -2 V, respectively. The swing of the control signal voltages SCAN1[n], SCAN2[n], EM1[n], and EM2[n] is -10 V to 5 V. C1, C2, and C_{OLED} are 100 fF, 200 fF, and 300 fF, respectively. The channel width and length of the driving TFT T1 are 3 μm and 6 μm, respectively, while the width and length of the remaining switching TFTs, T2 to T6 are 2 μm and 3 μm, respectively. The simulation is performed for the ultra high definition (UHD, 3840 × 2160) 4K display with a frame refresh rate of 60 Hz. Accordingly, the 1H time is set to 7.6 μs, and the reset, compensation, and data input periods are assigned 1H, 20H, and 1H, respectively.

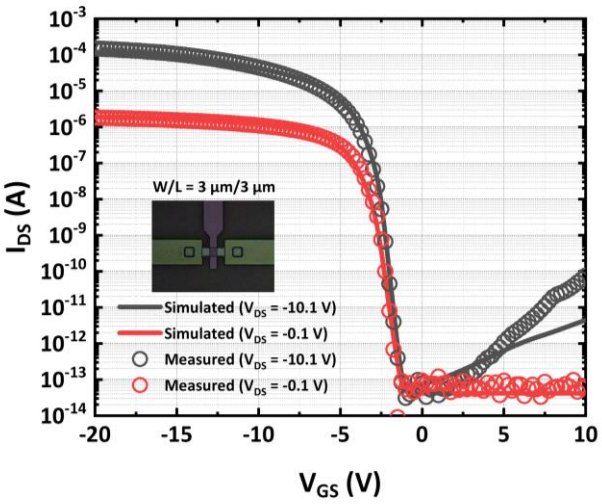

Figure 2. Simulated and measured transfer curve of the LTPS TFT.

Figure 2 shows the measured and simulated transfer curves of LTPS TFT with and aspect ratio 3 μm / 3 μm when gate-to-source voltage is increased from -20 V to 10 V and the source-to-drain voltages are -0.1 V and -10.1 V. The electrical characteristics of the LTPS TFT used in simulation are as follows: a V_{TH} of -4.41 V, mobility of 29.95 $cm^2/V•s$, and SS of 225 mV/dec. The OLED model used in simulation consists of two parallel junction diodes with a series resistor and a parallel capacitor, where the capacitor represents the capacitance of the OLED.

We conducted compensation simulations under three different conditions: V_{TH} variations, OLED turn-on voltage shifts, and ELVDD reductions. The turn-on voltage shifts of the OLED increased with stress time, showing a shift of 0.25 V after a stress time of 40,000 seconds [9], [10].

Figure 3. (a) shows node voltages of gate and source voltage of driving TFT T1 over period when the data voltage is -4 V. This confirms that the proposed pixel circuit can detect and compensate for deviation in the electrical properties of the driving TFT. Figure 3. (b) is a detailed view of the gate and source node voltages during the emission period under the conditions of ΔELVDD = -10% and OLED stress time = 40,000 s. This suggests that, despite deviations, the voltage difference between the source and gate remains constant during the emission period, allowing for a stable current output.

Figure 4. (a) shows the dynamic range of OLED current according to the data voltage, including different conditions. It shows that the OLED current exhibits a wide dynamic range of 80 pA to 112 nA when the data voltage ranges from -6 V to -1.5 V. Additionally, it confirms that a stable output is achievable even under varying conditions. The top graph in Figure 4. (b) shows the error rates of OLED current for V_{TH} variations of +0.5 V, -0.5 V, +1.0 V and -1.0 V. The maximum error rate in this case is 6.76% when ΔV_{TH} = -1.0 V and the data voltage is -5.25 V. The

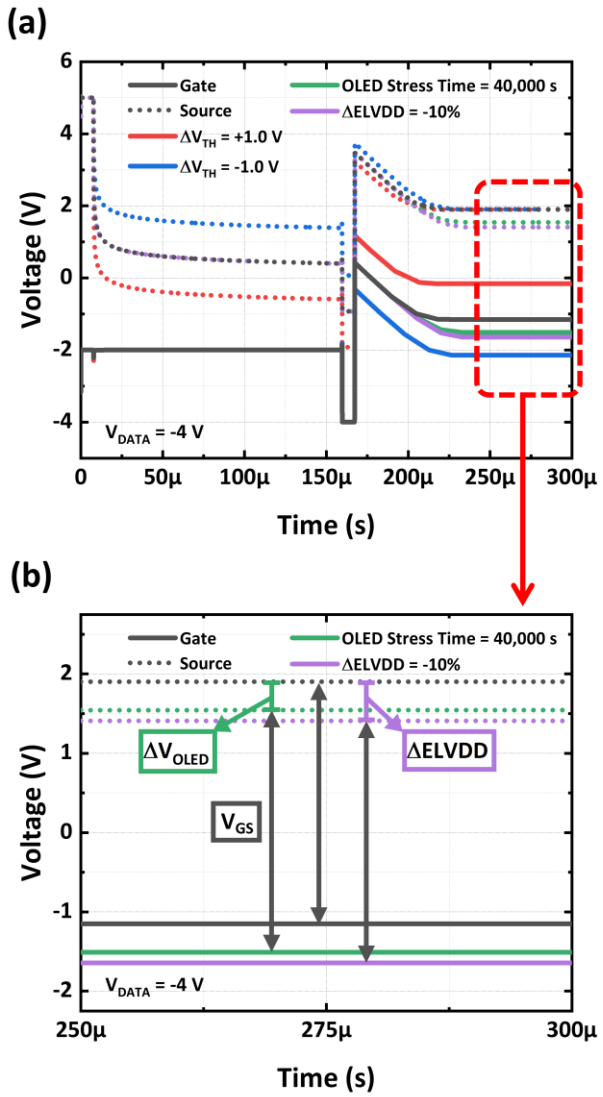

Figure 3. (a) Shows the simulation results of the gate and source node voltages of the driving TFT T1 when the data voltage is -4 V, and (b) is a detailed view of the node voltage during the emission period under the conditions of ΔELVDD = -10% and OLED stress time = 40,000 s

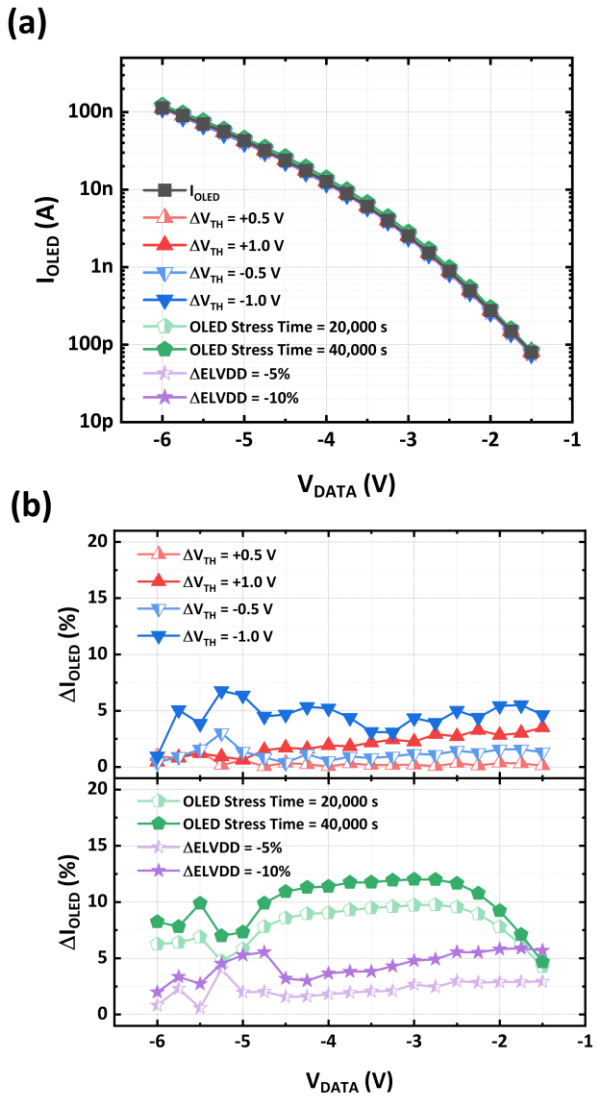

Figure 4. (a) Shows the OLED current according to the data voltage, and (b) shows the OLED current error rates according to the data voltage under the conditions of ΔV_{TH} = ±0.5 V, ±1.0 V, OLED stress time = 20,000 s, 40,000 s, and ΔELVDD = -5%, -10%.

bottom graph in Figure 4. (b) shows the error rates of OLED current under conditions where the OLED stress time is 20,000 s and 40,000 s and the ELVDD reduction is -5% and -10%. The maximum error rates for each condition are as follows: 12% when the OLED stress time is 40,000 s and the data voltage is -3 V, and 5.89% when ΔELVDD is reduced by 10% and the data voltage is -1.75 V. The current error rate for OLED degradation is better at low levels of current because the current in the degraded OLED model rises exponentially, resulting in larger deviations as the current rises.

Consequently, these results confirm that the proposed pixel circuit can stably outputs currents from 80 pA to 112 nA under various conditions with an error rate below 12% (under the conditions of an OLED stress time of 40,000 s and a data voltage of -3 V).

4. Conclusion

We propose a novel LTPS-based pixel circuit consisting of six LTPS TFTs and two capacitors. The proposed circuit successfully compensates for V_{TH} variations (±0.5 V, ±1.0 V), OLED degradation over time (20,000 s, 40,000 s), and ELVDD reductions (-5%, -10%). Therefore, we expect that the proposed pixel circuit will maintain stable OLED current levels under various conditions.

5. Acknowledgements

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