Micro-LED Pixel Circuit with Threshold Voltage Compensation Using a-IGZO TFT

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Abstract

Micro LED is undergoing extensive research as a leading next-generation display technology. Micro LED utilizes a Pulse Width Modulation (PWM) technique, where the pulse width is directly proportional to the sampled value of the signal. In this study, we successfully improved a pixel circuit that effectively compensates for both positive V_{TH} and negative V_{TH}. When the V_{TH} of the drive TFT controlling the PWM was shifted, the error rate ranged from approximately 0.3% to 0.6% for positive V_{TH} and 0.28% to 0.57% for negative V_{TH}. For the drive TFT controlling the CCG, the V_{TH} shift resulted in error rates of approximately 0.04% to 0.17% for positive V_{TH} and 0.04% to 0.11% for negative V_{TH}.

Author Keywords

Micro-LED, Pixel Circuit, a-IGZO, Threshold Voltage, PWM, TFT, Display

1. Introduction

Micro-LED is a Light Emitting Diode (LED) with a size of 100 µm or smaller [1]. Due to its low power consumption and excellent contrast ratio, it is considered a next-generation display technology. Currently, Micro-LED is known as a display that effectively addresses the shortcomings of Liquid Crystal Display (LCD) and Organic Light Emitting Diode (OLED), making it a promising industry for the future. Micro-LED demonstrates better performance in terms of response time, brightness, and contrast ratio compared to LCD. Furthermore, the inorganic compound-based Micro-LED has a longer lifespan than OLED, which is composed of organic compound layers that are highly sensitive and vulnerable to oxygen and moisture [2] [3]. OLED adjusts brightness by varying the current amplitude in its driving method. However, for Micro-LED, changes in current amplitude can alter the wavelength of light, causing color distortion on the display screen.

To prevent color distortion in displays with Micro-LEDs, a driving method must be used that maintains a consistent current amplitude while precisely controlling the emission time [4]. For this reason, most Micro-LED pixel circuits currently use Pulse Width Modulation (PWM), where the pulse width is proportional to the signal value. The electron mobility of amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) Thin Film Transistors (TFTs) is faster than that of Hydrogenated Amorphous Silicon (a-Si:H) TFTs. Additionally, a-IGZO TFTs exhibit higher uniformity than Low-Temperature Polycrystalline Silicon (LTPS) TFTs, making them highly suitable for large-area displays. Due to these advantages, a-IGZO TFTs are widely used in many display technologies. However, if a-IGZO TFTs degrade, such as through threshold voltage shifts, it can result in brightness inconsistencies and image distortion. [5].

This study aims to improve pixel circuits that compensate for both positive V_{TH} and negative V_{TH} .

2. Reference Pixel Circuit

Figure 1 shows a Micro-LED pixel circuit consisting of 10 TFTs and 2 capacitors. T1 to T8 are switching TFTs, and T9 and T10 are the drive TFTs for PWM and CCG. However, this pixel circuit has a problem where the V_{TH} value of the drive TFT does not compensate correctly when it is in a negative state.

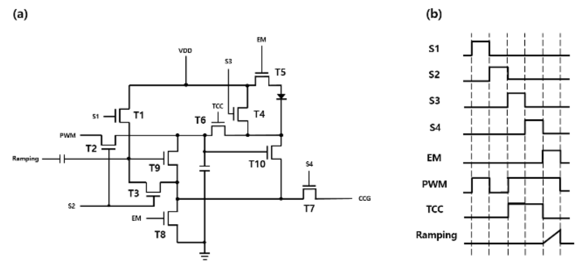

Figure 1. (a): 10T2C pixel circuit, (b): timing diagram

When the S1 becomes high, T1 is turned ON. At this time, the VDD voltage is stored at the gate of the driving TFT, T9. Due to the stored VDD voltage, T9 is turned ON.

When the S2 signal is at a high voltage, T2 and T3 are turned ON. The PWM voltage can then be applied to the gate of T9 through T2 and T3. During this process, the PWM voltage passes through the drain and source of T9. As a result, the gate voltage of T9 becomes PWM + V_{TH_T9}.

When the S3 signal and TCC signal are at high voltage, T4 and T6 are turned ON. At this point, the VDD voltage is stored at the gate of the drive TFT, T10. Due to the stored VDD voltage, T10 is turned ON.

Since the S4 signal is at a high voltage, T7 is turned ON. The CCG voltage can then be applied to the gate of T10 through T6 and T7, both of which are turned ON. During this process, the CCG voltage passes through the drain and source of T10. As a result, the gate voltage of T10 becomes CCG + V_{TH_T10}.

When the EM signal is at a high voltage, T5 and T8 are turned ON. At this time, current flows through the diode, initiating light emission. As the ramping signal increases, T9 is eventually turned ON due to the bootstrap effect. During this process, a low voltage is stored at the gate of T10. As a result, T10 is turned OFF, and light emission stops.

Figure 2 shows a simulation of the current values when the V_{TH} of T9, which controls PWM, is +3.2, +1.6, 0.0, -1.6, and -3.2 V. When V_{TH} is +3.2 and +1.6 V, the error rate relative to 0.0 V is approximately 0.004 %, confirming that compensation occurs. When V_{TH} is -1.6 and -3.2 V, the error rate compared to 0 V is approximately 2.18 to 4.55 %, confirming the effectiveness of the compensation

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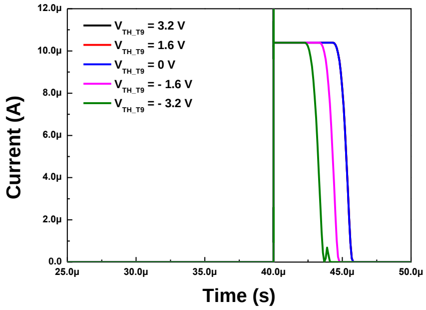

Figure 2. Current values when the threshold voltage values of T9 are +3.2, +1.6, 0, -1.6, and -3.2 V respectively

Figure 3 shows simulated current values when the V_{TH} of T10 is +3.2, +1.6, 0, -1.6, and -3.2 V, respectively. When V_{TH} is +3.2 V and +1.6 V, the error rate relative to 0 V is approximately 0.09%, confirming the effectiveness of the compensation.

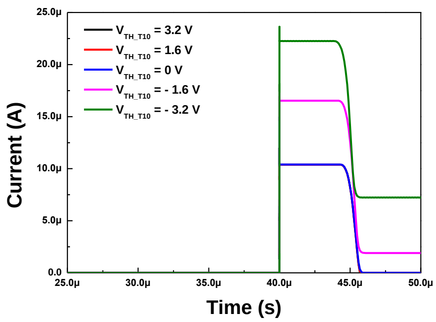

Figure 3. Current values when the threshold voltage values of T10 are +3.2, +1.6, 0, -1.6, -3.2 V respectively.

However, when V_{TH} is -1.6 and -3.2 V, the error rate relative to 0 V is approximately 58.8 ~ 114.01 %, confirming that compensation does not occur. Additionally, when the ramping signal increases and T9 is turned ON due to the bootstrap effect, the voltage at the gate of T10 does not drop below -1.6 V or -3.2 V. Consequently, during the light emission stop phase, the current does not drop to 0A.

3. Proposed Pixel Circuit

To address the issue of the pixel circuit's inability to compensate for negative V_{TH} voltages, a new pixel circuit is proposed, as shown in Figure 4.

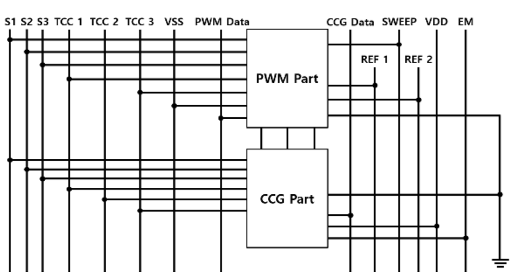

Figure 4. Schematic diagram of the newly proposed pixel circuit.

Figure 5 shows the gate node voltage waveform of the PWM drive TFT. The gate node voltages for V_{TH} values of +3.2, +1.6, 0, -1.6, and -3.2 V are -4.92, -6.41, -7.91, -9.41, and -10.91 V, respectively.

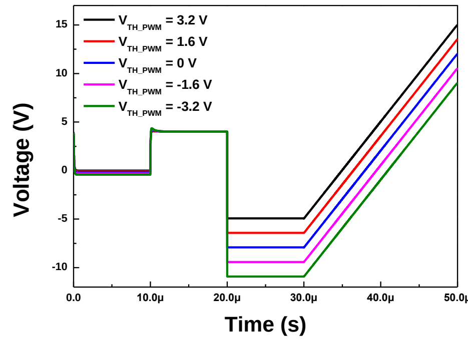

Figure 5. Gate Node voltage waveform of PMW drive TFT

These gate node voltage values are stored well with a consistent difference of 1.6 V corresponding to the threshold voltage difference. During the emission period (30 μs~50 μs), the Sweep signal gradually increases, and the gate node voltage rises due to the bootstrap effect.

Figure 6 shows the gate node voltage waveform of the CCG driving TFT.

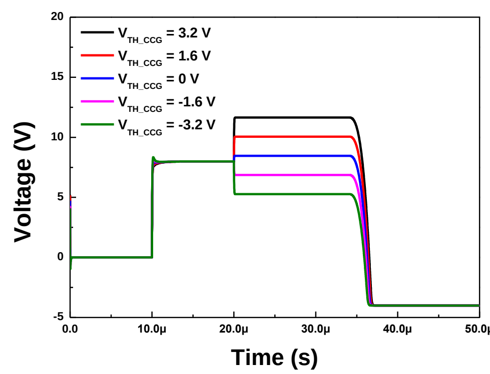

Figure 6. Gate Node voltage waveform of CCG drive TFT

The gate node voltage values for V_{TH} values of +3.2, +1.6, 0, -1.6, and -3.2 V are 11.65, 10.06, 8.5, 6.86 V, and 5.26 V, respectively. These gate node voltage values are stored well with a consistent difference of 1.6 V corresponding to the threshold voltage difference. During the 35 μs to 50 μs period, the bootstrap effect causes a voltage drop through the Turn ON PWM driving TFT, resulting in the cessation of light emission.

Figure 7 shows a simulation of the current values when the V_{TH} of the PWM driving TFT is +3.2, +1.6, 0, -1.6, and -3.2 V. For V_{TH} of +3.2 and +1.6 V, the error rate relative to 0 V is approximately 0.3 and 0.6 %, confirming compensation. For V_{TH} values of -1.6 and -3.2 V, the error rate relative to 0 V is approximately 0.28 and 0.57 %, confirming the effective compensation.

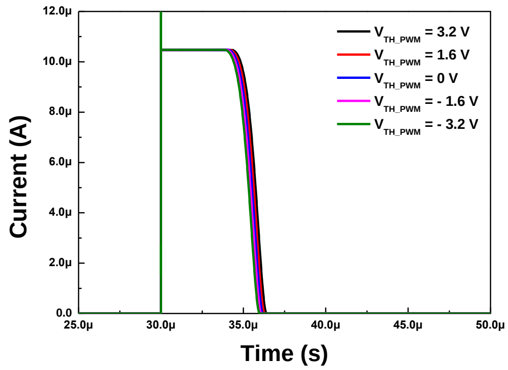

Figure 7. Current values when the threshold voltages of PWM drive TFT are +3.2, +1.6, 0, -1.6, and -3.2 V respectively

Figure 8 shows a simulation of the current when the V_{TH} of the CCG drive TFT is +3.2, +1.6, 0, -1.6, and -3.2 V. For V_{TH} of +3.2 V and +1.6 V, the error rate relative to 0 V is approximately 0.04 and 0.17 %, confirming compensation. For the V_{TH} of -1.6 and -3.2 V, the error rate relative to 0 V is approximately 0.04 and 0.11%, confirming the effective compensation.

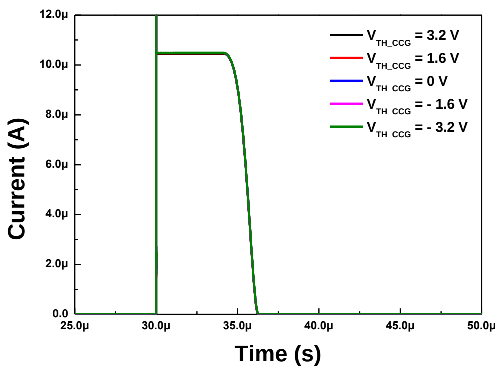

Figure 8. Current values when the threshold voltage of CCG drive TFT are +3.2, +1.6, 0, -1.6, and -3.2 V respectively

Additionally, by using a lower VSS signal, such as -1.6 V or -3.2 V, instead of GND, the issue of the current not dropping below 0A during the emission stop phase, as shown in Figure 3, is effectively prevented.

Figure 9 illustrates the emission times of a Micro-LED as the PWM voltage changes. When the PWM voltages are -5, -7, -9, -11, and -13 V, the corresponding emission times are 1.437, 3.326, 5.215, 7.104, and 8.993 µs, respectively. This simulation result confirms that the emission time can be modulated using pulse-width control via the PWM voltage.

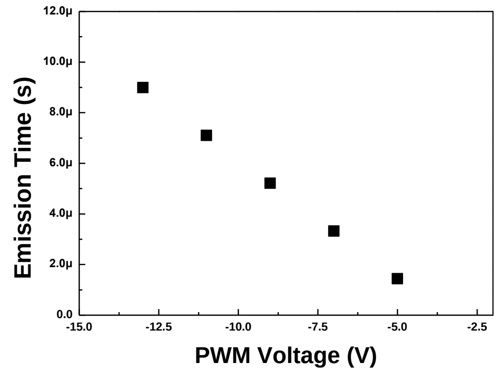

Figure 9. Micro-LED light emission time when PWM voltage are -5, -7, -9, -11, and -13 V.

Figure 10 shows the current values of a Micro-LED as the CCG voltage varies. When the CCG voltages are +12.3, +11.3, +10.3, +9.3, and +8.3 V, the corresponding current values are 14.702 µA, 14.006 µA, 13.105 µA, 11.934 µA, and 10.472 µA, respectively. This simulation result confirms that the current values can be modulated using pulse-amplitude control via the CCG voltage.

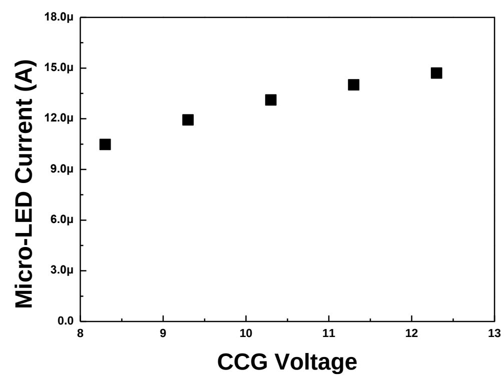

Figure 10. Micro-LED current values when CCG Voltage are +12.3, +11.3, +10.3, +9.3, and +8.3 V

Figure 11 shows the emission times of a Micro-LED when the V_{TH} of the PWM-driven TFT is +3.2, +1.6, 0, -1.6, and -3.2 V. When the PWM voltage is -9 V, the emission times are 5.353 µs, 5.241 µs, 5.139 µs, 5.039 µs, and 4.937 µs, respectively. When the PWM voltage is -11 V, the emission times are 7.241 µs, 7.13 µs, 7.028 µs, 6.928 µs, and 6.826 µs. When the PWM voltage is -13 V, the emission times are 9.131 µs, 9.019 µs, 8.917 µs, 8.817 µs, and 8.715 µs.

Figure 12 illustrates the current values of a Micro-LED when the V_{TH} of the CCG-driven TFT is +3.2, +1.6, 0, -1.6, and -3.2 V.

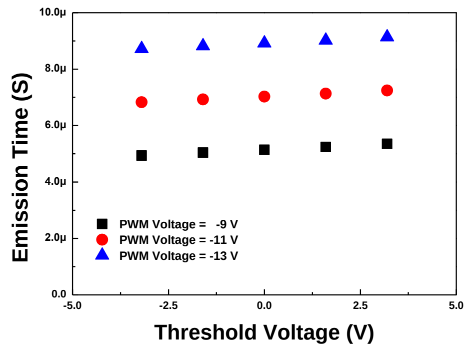

Figure 11. Micro-LED light emission time when threshold voltages are +3.2, +1.6, 0, -1.6, and -3.2 V

When the CCG voltage is +8.3 V, the current values are 10.458 µA, 10.471 µA, 10.476 µA, 10.481 µA, and 10.487 µA, respectively.

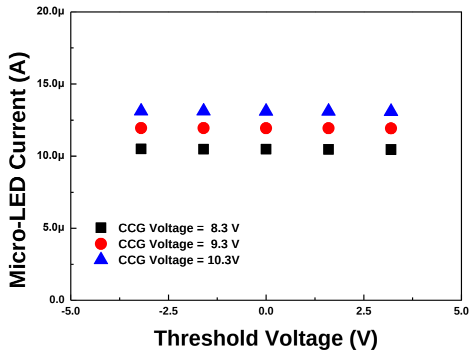

Figure 12. Micro-LED current values when threshold voltages are +3.2, +1.6, 0, -1.6, and -3.2 V

When the CCG voltage is +9.3 V, the current values are 11.922, 11.933, 11.937, 11.941, and 11.947 µA. Lastly, when the CCG voltage is +10.3 V, the current values are 13.096, 13.104, 13.107, 13.11, and 13.115 µA.

4. Conclusion

The oxide TFT pixel circuit proposed for micro-LED which could compensate for both the positive V_{TH} and negative V_{TH} values. When the V_{TH} of the PWM driving TFT is +3.2 V and +1.6 V, the error rate relative to 0 V is approximately 0.3%~0.6%. When the V_{TH} is -1.6 V and -3.2 V, the error rate relative to 0 V is approximately 0.28%~0.57%. For the CCG driving TFT, when the V_{TH} is +3.2 V and +1.6 V, the error rate relative to 0 V is approximately 0.04%~0.17%. When the V_{TH} is -1.6 V and -3.2 V, the error rate relative to 0 V is approximately 0.04 to 0.11%.

5. References

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