Layout Optimization of AMOLED Pixel Circuits based on Deep Reinforcement Learning

Yeonhak Pyo[1], *Hyeonseong Cho*[1], *Taewoong Lee*[1], *Byeonggeon Ko*[2], *Taehyun Kim*[2], *Hyoungsik Nam*[1]

[1]**Dept. of Information Display, Kyung Hee University, Seoul 130-701, Korea**
[2]**Display Research Center, Samsung Display Co., Ltd, Korea**

Abstract

As high-resolution AMOLED pixel circuits have become more complex, the automation for the circuit design process has been strongly demanded. In this paper, a reinforcement learning-based framework is proposed to optimize the area of the pixel circuit layout by iteratively device repositioning and connection rerouting, leading to significantly improved time and cost efficiency.

Author Keywords

Layout optimization, deep reinforcement learning, AMOLED, pixel circuit.

1. Introduction

As the display industry evolves rapidly, active-matrix organic light-emitting diode (AMOLED) panels require high resolution, superior image quality, and low power consumption that increase the complexity of pixel circuit design. [1] In a single pixel area, several devices such as driving thin-film transistor (TFT), switching TFTs, and capacitors should be placed under consideration in vertical and horizontal symmetry across the panel. Moreover, the layout must comply with design rules to be stably adapted to the manufacturing process. These challenges make the design process more complicate.

Most of this complicated design process relies on the skilled engineers, resulting in significant time and cost. Therefore, it is important to assist or automate the pixel circuit design including circuit structure [2] as well as layout. For this purpose, Design Space Explorer (DSE) [3,4] has been proposed, which generates a high-resolution layout by exploring various placements and routings. DSE has shown the possibility of automating the initial design while minimizing interference or parasitic capacitance problems between signal lines. Through this, the design rules of the manufacturing process can be verified in real time and finally converted to a graphical design system (GDSII) to support a smooth design process.

However, the existing DSE method has limitations in that it has a long search time and can't completely solve the problem caused by the reduced distance between signal lines. This problem is especially evident in ultra-high-resolution AMOLED panels as pixel unit areas shrink, making it difficult to efficiently address it using manual design methods.

In this study, we propose a reinforcement learning (RL) based framework that performs additional exploration and optimization on the initial layout generated by the existing DSE. In the first step, DSE generates the initial layout by adjusting the positions and rotations of signal lines and elements. In the second step, the RL framework receives the initial layout, selects element movement directions through agents, and optimizes them by rearranging and routing them in the environment. The RL model dynamically adapts to complex constraints by iteratively refining layouts based on feedback from performance metrics such as area reduction, and compliance with design rules.

This approach can achieve a higher level of layout quality in a shorter time than conventional methods. This paper will demonstrate that the proposed framework can improve the time and cost efficiency of AMOLED pixel circuit design.

2. Proposed Layout Optimization Framework

2.1 Overall Architecture

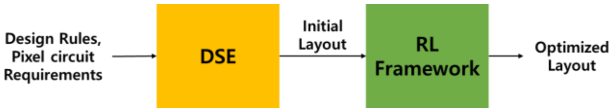

Figure 1. Overall Layout Optimization of Pixel Circuits Framework architecture.

The proposed framework for layout optimization of pixel circuit requires DSE and RL model as shown in Fig. 1.

First, we use DSE to automatically construct an initial layout through exploration based on design rules and pixel circuit requirements. Then, we input the initial layout into the RL model to perform additional exploration and optimization and output an optimized layout.

2.2 Design Space Explorer

DSE is a layout optimization methodology developed to address challenges in achieving high-resolution designs in OLED displays. It focuses on optimizing the placement and routing of signal lines, devices, and contact points (CNTs) to overcome issues such as parasitic capacitance, signal interference, and extended search times. DSE systematically explores various configurations by changing the location and rotation of signal lines and devices as shown in Fig. 2, enabling the creation of high-resolution layouts. However, traditional methods face limitations due to the exponential growth of search space, which can result in billions of possibilities for pixel structures and require significant computational time. To address this, predictive models are integrated into DSE to prioritize high-resolution layouts by analyzing factors such as route direction, CNT count, and dispersion.

The predictive model allows DSE to estimate route results without performing full routing simulations. By converting circuit netlists into graphs, the model predicts route connection directions for each device and evaluates CNT numbers and variance. Metrics like Half Perimeter Route Length (HPRL) are used to approximate route lengths efficiently. This approach significantly reduces execution time, enabling results within days rather than months. Additionally, DSE minimizes parasitic

ISSN 0097-996X/25/5603-1635-$1.00 © 2025

capacitance by optimizing CNT dispersion, which reduces metal density and improves signal integrity. Congestion maps are also employed to avoid routing overlaps and distribute routes evenly across the layout.

DSE's ability to generate high-resolution layouts has been experimentally validated. Comparative analysis with reference designs demonstrated an average consistency of 95.4%, with improvements in metal density (10%) and reductions in parasitic capacitance (15%). The methodology streamlines the design process by converting results into Graphic Design System (GDSII) format for seamless integration with existing workflows. Overall, DSE represents a significant advancement in layout design for modern display technologies, reducing development time and costs while enhancing performance.

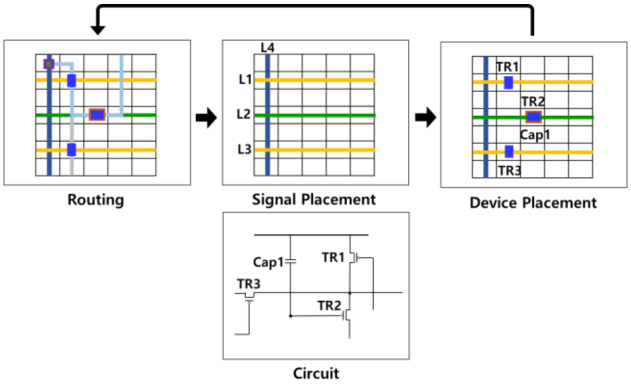

Figure 2. DSE process.

2.3 RL Framework

The RL framework shown in Fig. 3 operates as follows:

1) Data layout change receives GDSII data of an initial layout from the DSE that is converted into a data format suitable for the RL framework.
2) The agent receives the converted initial layout data (initial state), which then selects an action based on its policy and delivers it to the environment.
3) The environment executes the action, computes the reward, and returns the new state and reward to the agent.
4) The resultant transition (state, action, reward, next state) is stored in its replay memory and used to update the parameters of its Q-network.
5) The state is renewed with the next state received from the environment, and the agent continues to take actions based on this updated state.
6) Steps 3) to 5) are repeated until the episode ends, and this process is iterated for a predefined number of episodes.
7) After completing all episodes, the RL framework outputs an optimized layout as the final result.

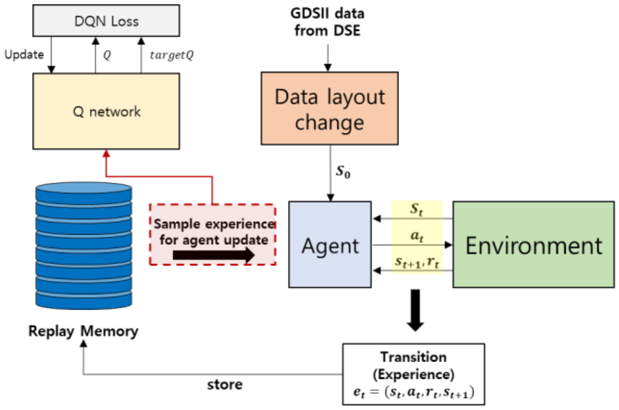

Figure 3. Overview of the proposed RL framework.

Data layout change. The coordinates of TFT, capacitor, contact, and routing are extracted from the GDSII data of the layout received from DSE and converted into data that can be used in the RL framework. GDSII data consists of coordinates that constitute each element, and among these coordinates, only the upper left and lower right coordinates of the square are separated by layer and converted into a form that can be used in the RL framework and transmitted to the agent.

Agent. The initial state received from the Data layout change is input to the deep neural network and an action is decided as depicted in Fig. 4. The state is transferred to the agent by separating it into several channels of TFT, capacitor, contact, and routing as illustrated in Fig. 5. In the case of the action, in order to consider all actions of moving left or right for each device, it has an action space corresponding to twice the total number of devices (TFT, capacitor, contact). The action output in this way obtains the reward and next state through the environment, and these are stored in the replay memory and used to learn the Q network.[5]

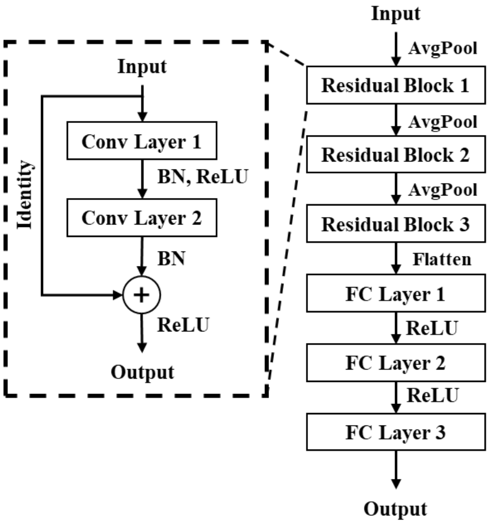

Figure 4. An architecture for the agent network.

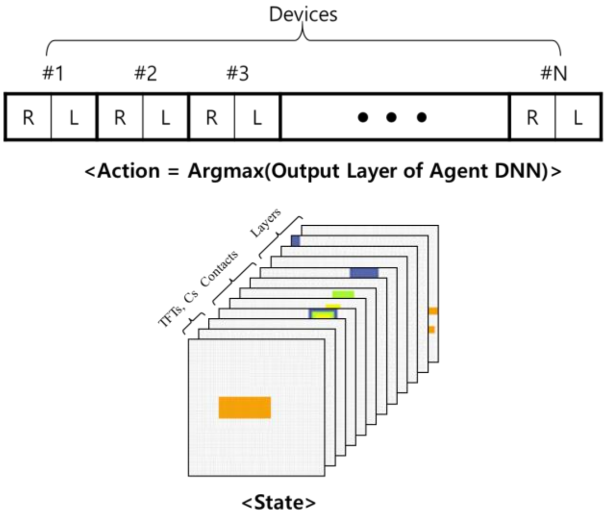

Figure 5. Action and state definition of the RL framework.

Environment. It receives an action from the agent and provides a new state and reward to the agent. First, it checks the device to move and the direction in which the device will move according to the input action. It verifies whether the device selected for the action and other devices and routings connected to this device in the upper and lower directions can move within a range that does not violate the design rule. If movement is impossible, the system outputs a penalty reward. On the other hand, if movement is possible, the device is moved and a compression process is performed so that all devices are compressed downward as much as possible while complying with the design rule. The reward is calculated based on the compressed area. If the area decreases, the reward is calculated in proportion to the decrease, and if there is no change in the area, the reward is calculated as 0 and the episode continues. If the area increases, a reward corresponding to the penalty is paid and the episode ends. The finally calculated reward and the new state after the action are stored in the replay memory and used for agent learning.

3. Results and Discussion

To evaluate the effectiveness of the proposed RL framework, we used a pixel circuit shown in Fig. 6(a) that consists of 5 TFTs without capacitors.

The results demonstrate that using the RL framework significantly improves area reduction compared to the input layout generated by DSE as presented in Fig. 6(b) and (c). The RL framework optimizes the layout by moving devices along the long axis and compressing them along the short axis, leading to a more compact layout. Table 1 provides a quantitative comparison of area reduction rates: while the compression only along the short axis achieves a reduction rate of 36.9%, the whole RL framework increases the reduction rate to 47.3%. These findings highlight the effectiveness of this RL-based optimization.

In addition, Fig. 7 demonstrates the dynamic learning process of the RL agent by showing the area reduction rate over sim, where 1 sim is equal to 10 episode and the target deep neural network of the agent is updated every sim. The learning curve exhibits fluctuations during training, with periods of improvement followed by occasional regressions. The overall increasing trend indicates steady improvement in area reduction rates as training progresses.

The computational time required for training is approximately 23 hours. While this duration demonstrates that RL-based optimization is computationally intensive, it remains feasible for practical applications given its significant performance gains.

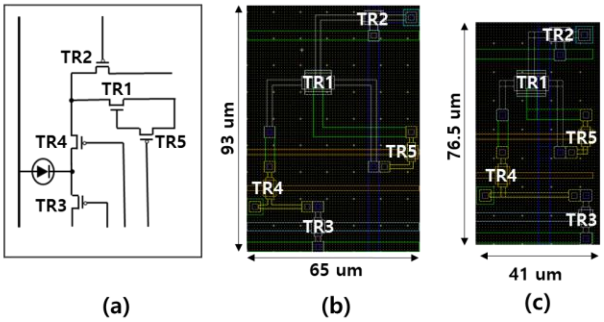

Figure 6. Evaluation results of the proposed RL framework. (a) Pixel schematic (b) Input layout (c) Output layout.

Table 1. Area reduction ratio of test layout

	Compression only at short axis	Whole RL framework
Area reduction ratio (%)	36.9	47.3

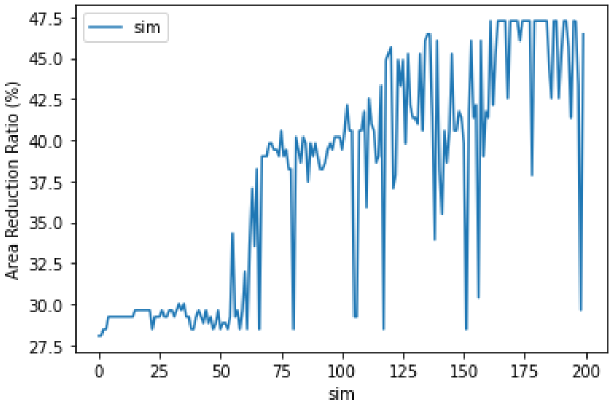

Figure 7. Pixel area reduction plot during the training period. 1 sim is equal to 10 episodes.

4. Conclusion

This study proposes a RL-based pixel circuit design automation framework and presents a novel approach for reducing the area of an AMOLED pixel circuit layout. The RL framework adopts a dual-stage structure that performs additional exploration and optimization after the initial layout generation of the existing DSE method. DSE generates the initial layout based on design rules and pixel circuit requirements, and the RL framework receives the initial layout and selects the movement direction of layout elements through a RL agent and optimizes rearrangement and routing within the environment. A RL framework dynamically adapts to complex constraints by repeatedly reflecting feedback based on performance indicators such as area reduction and design rule compliance. Through this, it is demonstrated that it can generate higher quality layouts in a shorter time than existing methods. In particular, the effectiveness of the framework is confirmed by 47.3% area reduction in the layout of a pixel circuit example.

5. Acknowledgements

This work was supported by Samsung Display Co., Ltd. and the Brain Korea 21 Four Program.

6. References

1. W. Jeong, et al. Low-power technologies for displays. Nature Reviews Electrical Engineering, 2025.
2. H. Cho, et al. PixelAI: Designing AMOLED Pixel Circuits using Reinforcement Learning. SID Symp. Dig. Tech. Papers, 2024
3. T. Kim, et al. A High Resolution Design Methodology for Organic Photo Diode Sensor Integration. SID Symp. Dig. Tech. Papers, 2024
4. J. Bang, et al. A High Resolution Design Methodology for Pixel Layout Generator. Proc. IMID, 2024
5. K. He et al. Deep Residual Learning for Image Recognition., Proc. IEEE CVPR. 2016, 770–778.