A New LTPS Pixel Structure to Improve the 1Hz Low-Brightness AOD Flicker Effect

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Abstract

In order to solve the problem of improving the wearable AoD performance of LTPS at 1Hz, the new process structure and pixel design of 3Mo1TiAlTi are used, and the new driving method can be used to achieve the observation of the 1Hz dial of LTPS wearable products at a visual distance of more than 15cm, without flicker.

Author Keywords

LTPS;1Hz;AoD; low-brightness;Mo;Cst

1. Introduction

With the development of display, green environmental protection and low power consumption have become an important basis for everyone's choice, especially the AoD mode of wearing, which requires the screen to display around the clock, and the screen display of 5Hz or even 1Hz is becoming more and more common, and the flickering problem caused by the low-frequency display must be solved; At present, LTPO technology is mainly used in the industry for 1Hz products, and the corresponding T3 and T4 tubes are changed to IGZO to reduce leakage, so as to maintain the Cst in the low-frequency stage and avoid flicker; At present, because T3T4 is LTPS TFT, the Cst leakage situation is still serious at 1Hz, especially in the case of low brightness, it is impossible to achieve visual flickering. In order to solve this problem, the new process structure and new pixel design of 3Mo1TiAlTi are used, and the new driving mode can be used to achieve the observation of the 1Hz dial of LTPS wearable products at a visual distance of more than 15cm, and all kinds of UI will not flicker.

2. Results and Discussion

First of all, the pixel circuit uses the function of Vref initialization DTFT on the basis of the special pixel circuitry, and the two capacitors of the circuit are also about Cst+C2=350fF. The process structure is 10mask process: PSI/M1(Mo)/M2(Mo)/ILD1/M3(Mo)/ILD2/M4/PLN/Anode/HTM, in which M1M2M3 is metal Mo, M4 is metal Ti/Al/Ti, and the pixel circuit is designed as special circuit Vref circuits and two large Cst capacitors can be designed, and Ti/Al/Ti is mainly used for designing data and VDD, and the wider and simpler Ti/Al/Ti design can provide better brightness requirements and optimize the bias of the role. For the drive, we use the special pixel circuitry+ Vref driving method. In the end, we got a 1.7Xinch, 3000nit, 360PPI real RGB, low-brightness AOD effect of 0.5nit 100% APL to achieve about -50dB, the same LTPO AoD effect LTPS wearable product. The capacitance values of C1 and C2 can be adjusted at will, and the ILD1 process can be optimized when the capacitance demand is about Cst+C2=200fF, and it can be made with only 9mask.

Special pixel circuits have multiple devices and capacitors, let's take the following pixel circuits as an example（Figure 1）, write normally when writing frames, do not write when holding frames, only initialize DTFT to relieve stress, Cst's leakage critical path between T8 and T10 node capacitance C2, Cst and C2 can be enlarged so that the hold frame can maintain G point voltage.

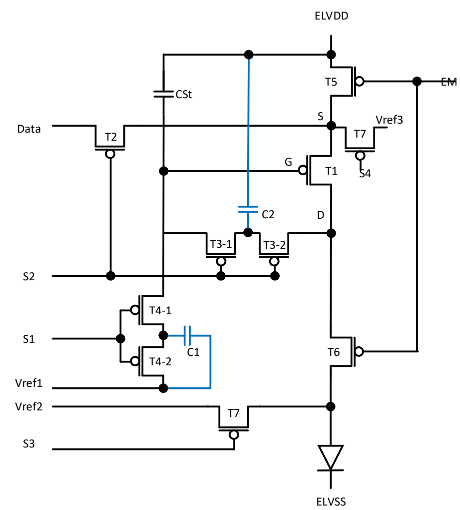

Figure 1 Pixel circuit diagram (an example)

According to the specific parameters, it can be seen that the parameters of the new circuit structure can be used to ensure the stability of voltage and current. When the brightness drops to 5nit, the current can still be kept in a stable state to avoid flickering.（Figure 2）

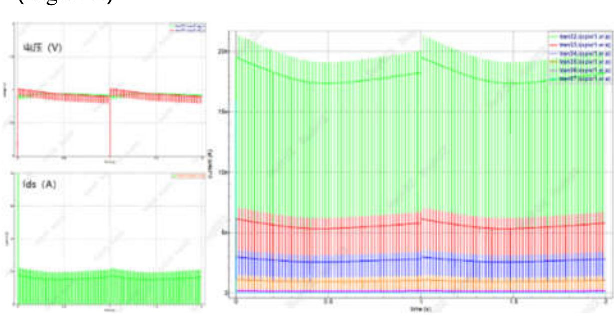

Figure 2 Simulation

In the specific process, we have greatly adjusted the thickness of each layer, reduced the thickness of ILD1, and increased the ILD2 layer, and the thickness of the film layer is between 1000~1500A. This warrants a larger capacitance design (Fig 3-1). In the design process, there are also more schemes for ILD1 and ILD2, and the

ISSN 0097-996X/25/5603-1410-$1.00 © 2025

small number of vias can add more space to design Cst or routing, etc., we use part of the sleeve hole optimized into one hole (Fig 3-2), ILD1+ILD2 film thickness is about 3500A, so that the etching depth of ILD2 directly etched to M2 metal layer is smaller, and the impact on the CD and dry engraving capacity of the hole is small.

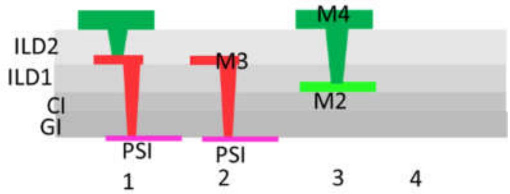

Figure 3-1 Pixel via cross-sections

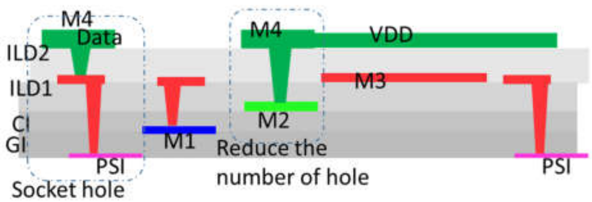

Figure 3-2 Sleeve hole reduction cross-sectional view

Considering the overall inorganic coating layer, it can be considered not to use ILD1 etching, only ILD2 etching, and such an inorganic coating layer can be etched into a 9mask process (Fig 4) using one mask at a time, that is, PSI/M1(Mo)/M2(Mo)/M3(Mo) /ILD/M4/PLN/Anode/HTM. This solution is suitable for designs with Cst+C2 within 200 fF or less than 360 PPI (real RGB).

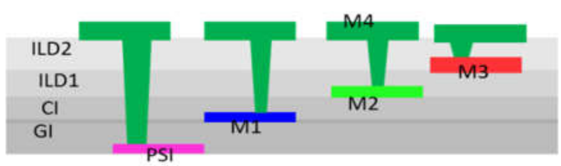

Figure 4 Pixel via cross-sections of 9mask

Specifically, M1 and part M3 are Cst gates, and M2 and M4 are Cst VDD electrodes. Part of M3 is a C2 gate, and M2 and M4 are C2 VDD electrodes (Figure 5).

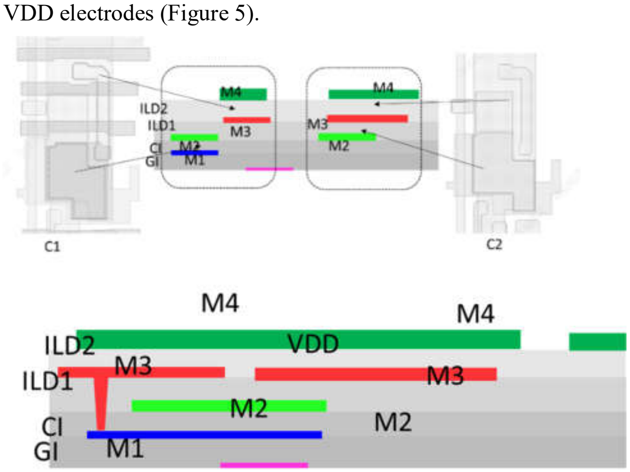

Figure 5 Capacitor structure cross-section

The area of the two M3s on M2 is changed to the capacitance adjustment of Cst and C2, and Cst and C2 can be designed with different proportions according to the requirements. Similarly, since most of the pixel connections use M3, M4 can be used to design data and VDD, and VDD can be designed with a larger width, and a larger width can correspond to a larger capacitance and a smaller voltage drop. The highlight uniformity of the product can also be guaranteed. In the specific production process, because the ILD2 film layer is thin, it is necessary to pay attention to prevent the trace of M3 in the M4 area during the dry engraving process of M4, and the optimal M3 is preferentially designed below M4. Or the ILD2 layer is appropriately thickened to 1500A. Our driver circuitry has also been changed to support the pixel circuit and structure.

3. Results and verification

In view of the above analysis and discussion, we have studied the actual fabrication of the two structures, and it can be found that the insulation layer between VDD and M2 as VDD as one pole of the capacitor, and M1 and M3 as the pole of the gate, can be set to be very thin to about 1000A, and the final Cst is very large.

We can see the 10mask process structure (Fig. 6.), Cst can reach a four-layer structure, and the half-engraved hole used connects M3 to PSI via M4, which is the pixel G-dot. Finally, we need to mainly etch when the ILD reaches M3 earlier, causing over-etching, and M3 cannot be too thin.

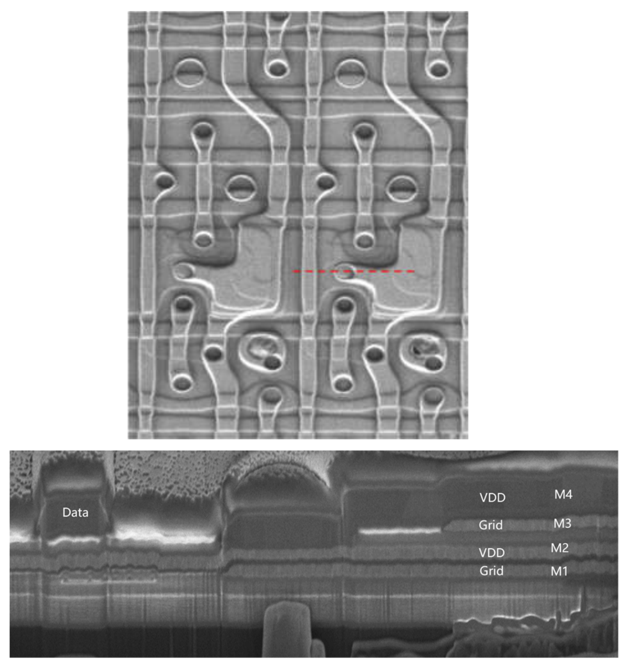

Figure 6 1PEP Via process structural

For the use of ILD1 and ILD2 vias (Fig.7.) , the process etching time is also more flexible, and it is more convenient to adjust the CD and taper angles of the two vias, and at the same time, ILD2 can be compatible with the ILD2 process in the flexible etching bending region.

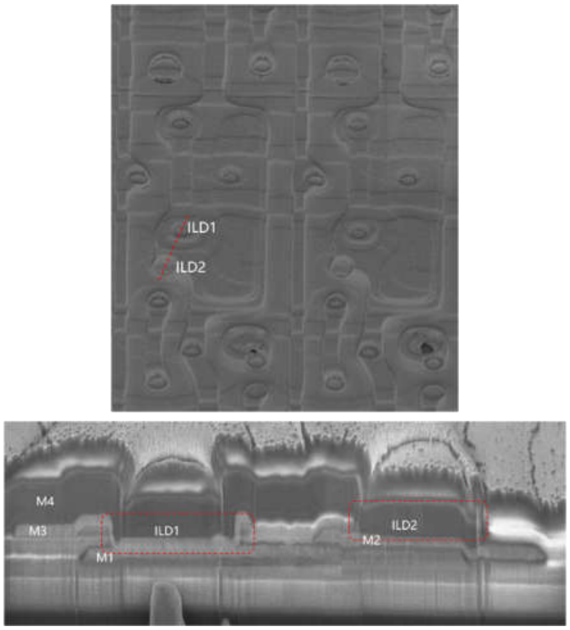

Figure 7 2PEP Vias process structural

Through verification, it is found that the capacitor layout space formed by M3 and M4 can break through the DTFT range and be designed to most of the pixel space（fig.8.）. This undoubtedly makes it possible to design larger capacitors for Cst and C2.

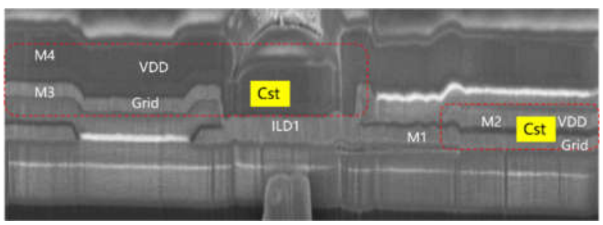

Figure 8 The space of Cst design

4. Impact of the Research

In the end, we use a new process and pixel structure layout, so that the product can be made in the case of 10mask or even 9mask LTPS process, The test result is about -50dB at 1Hz, 0.5nit, 100% APL，and the AOD effect of the product can reach the level of LTPO. The LTPS wearable product reaches 1Hz, and the dial can be observed at a visual distance of more than 15cm, and all kinds of UI are not flashing.

5. References

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