Novel Scan Driver Circuit and Power Consumption Reduction Structure for Oxide-Based OLED Display

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Abstract

To reduce the power consumption of OLED display, we focused on the power consumption of gate drivers. In this study, we present a novel circuit structure of data scan driver and methods of reducing power consumption. We fabricated 600 stage scan driver array and achieved reducing 69.7% of data addressing scan driver.

Author Keywords

Gate Scan Driver; Low Power Consumption; Fast Falling Slew Rate;

1. Introduction

The adoption of OLED panels, which started with mobile devices, is growing into Mid-Size devices including tablet PCs and laptops. From 2024 to 2028, shipments of OLED panels for Laptops and Tablets are expected to increase 18.5% annually to 34.8 million units [1]. The fast response speed of OLED panels is a big advantage in the gaming laptop market and is appealing to consumers who demand accurate color expression such as designers and video editors. However, the power consumption of OLED panels does not meet the customer's expectations in a specific environment. Moreover, the popularization of On-device AI such as Samsung Electronics' Galaxy AI [2-3], which was released in 2024, is further complicating the problem of power consumption. Due to the characteristics of On-device AI service, high-performance chips perform high-operation tasks, leading to high power consumption.

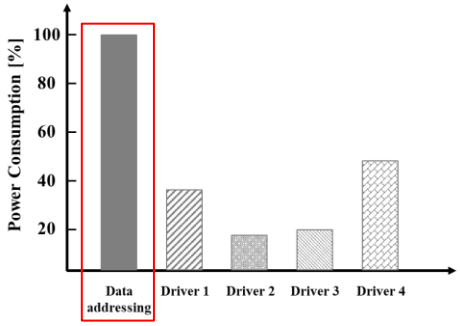

Figure 1. Power consumption ratio of the 14-inch oxide integrated gate driver

The largest part of power consumption of OLED display is emission power [4]. However, as panel driving frequency increases, power consumption of integrated gate driver also increases due to higher clock frequency. Among integrated gate drivers, Data Addressing (DA) scan driver, which writes data voltage, has the highest power consumption ratio of about 44.5 % running at 120 Hz. In this paper, a novel structure is proposed for the DA scan driver, and a study to reduce power consumption based on the proposed circuit is to be mentioned

2. Novel Scan Driver Circuit Structure

2.1. 1H Overlap Driving Method

In display operation, 1H time is the time allocated to write the data voltage to the horizontal line of one line in the direction of the gate line of the active area. The calculation of 1H time is the same as the following equation.

$$1H = 1\ [s] / Frequency\ [Hz] / Resolution\ [line] \quad (1)$$

The ideal DA pulse is a right-angled waveform, which outputs a high voltage at the start of the allocated 1H time and a low voltage at the end of the 1H time. However, in the actual panel, the resistance component and capacitance component cause RC delay. For this reason, there are Rising Time Delay (t_r), which is the time when the DA pulse rises to the high voltage, and Falling Time Delay (t_f), which drops to the low voltage, and this time reduces the effective 1H time. 1H time shortens with the increase of driving frequency and higher resolution. To maximize 1H time, the 1H overlapping driving method is introduced. Overlap Driving is a driving technique that raises the gate line to high state before addressing the data voltage so that the gate line is already turned on when addressing the data voltage. When overlap driving is operated, t_r time does not affect 1H time, and only t_f time determines the actual 1H time.

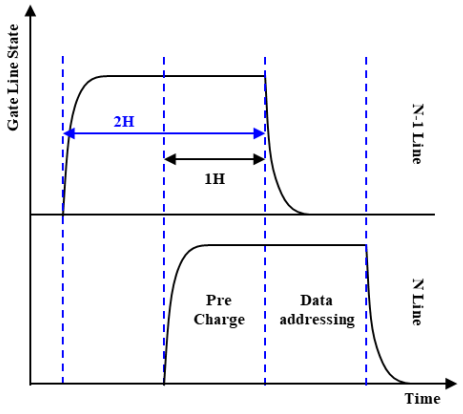

Figure 2. A graph showing the state of the gate line when the 1H overlap of the N-stage and N-1 stage is operated. The data voltage is written at the data addressing timing.

2.2. Dual path discharge structure of the proposed Scan Driver

In conventional scan driver structure, the clock line is connected to the buffer TR [5]. The buffer TR charges and discharges the gate line. As a result, width of buffer TR determines rising time and falling time. However, as the buffer TR increases, the parasitic cap capacity due to the physical TR size also increases, so increasing the TR width is not an effective method.

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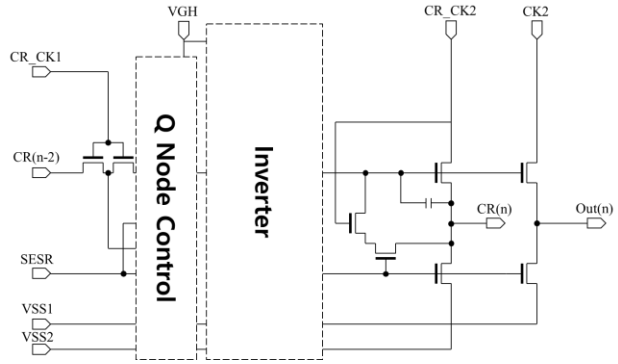

Figure 3. Example of a conventional Scan Driver. Includes the Carry Signal Line and the Carry Clock Line

To minimize falling time, we propose the dual path discharge structure by adopting pull down TR which the gate is connected to the CR(N+2) signal. As the falling of output signal begins at the same time of CR(N+2) rising, buffer TR and pull down TR discharges the gate line simultaneously. By using this method, falling time can be decreased effectively.

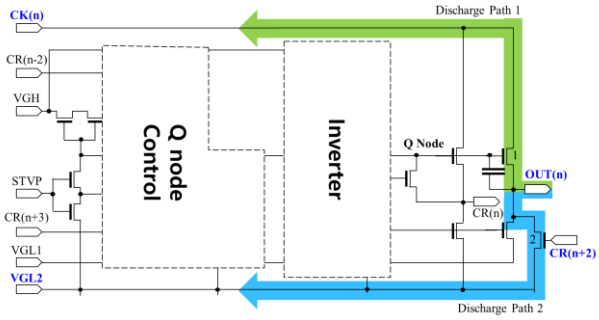

Figure 4. Structure of the novel DA Scan Driver. When the gate line is discharged, the Dual Path Discharge structure is adopted and discharged to Path 1 and Path 2 at the same time.

2.3. Carry Clock Less Structure

Conventional DA Scan Driver consists of a 'Carry Signal Line' for triggering the next stage and a 'Carry Clock Line' for charging and discharging the Carry Signal Line. The reason why the Carry Clock Line is used separately without operating the carry with the DA Clock Line is that the DA Clock Line directly charges and discharges the Active Line. If the load of the Carry Signal Line is added to the DA Clock Line, a problem occurs that leads to the delay t_r, t_f of the DA clock pulse. At this time, the structure that uses the Carry Clock Line separately for the carry logic operation can reduce the load burden of the DA Clock Signal, but it is disadvantageous to save power consumption because an additional Clock Signal Line is used. To overcome this, the novel DA Scan Driver introduced the Carry Clock Less structure. The novel DA driver uses the carry signal of N-2, N+2, and N+3 as its logical operation. Pre charge the Q node through N-2 carry and control the Pull Down TR T2 through N+2 carry. After that, the Q node is discharged to VSS1 level through N+3 Carry. By deleting the Carry Clock Line, the power consumption due to the Carry Clock was removed.

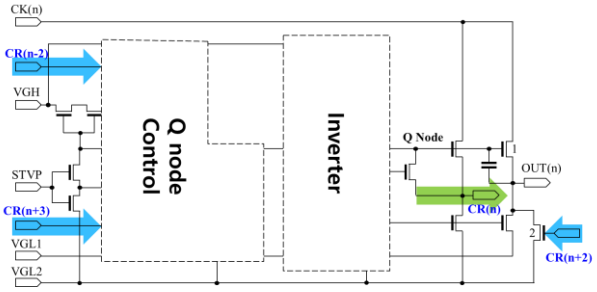

Figure 5. Pre-charging the Q node through the N-2 Carry signal and holding it to the VSS2 level through the N-3 Carry signal. N+2 Carry is used as DA Line Discharge.

3. Scan Driver Power Reduction Methods

3.1. About Carry Clock Power Consumption

The power consumption of the Display Scan Driver is calculated by the following equation, which is called Dynamic Power consumption.

$$P_{dynamic} = C_{parasitic} \times V^2_{swing\ range} \times f_{period} \quad (2)$$

As mentioned in Section 2.3, the conventional driver circuit uses two types of clocks, CR_CK and CK, for the carry clock line and the carry signal line. Since the two clock lines are separated, the load of the CK is reduced, which helps to improve the falling time. However, since each of the two types of CK lines has the same dynamic power consumption as Equation (2), it is disadvantageous to power consumption. In this paper, the power consumption of the novel circuit was improved by removing the Carry Clock line, and the falling time was also guaranteed through the dual path discharge structure.

3.2. Buffer TR Down Sizing

The DA Scan Driver is connected to the drain node of the buffer TR because the clock directly transfers the active line to the high state for 1H time. Even when the allocated time is not 1H, the clock line switches the high voltage and low voltage. At this time, the parasitic capacitance between the gate node of the buffer TR and the drain node to which the clock is connected leads to unnecessary power consumption of the DA Scan Driver. In order to reduce the parasitic capacitance of the gate node and the drain node of the Buffer TR, down-sizing of the Buffer TR is required, but down-sizing of the Buffer TR delays the rising time and falling time of the DA output waveform. In conclusion, the size of Buffer TR and the power consumption of Scan Driver are in a trade-off relationship.

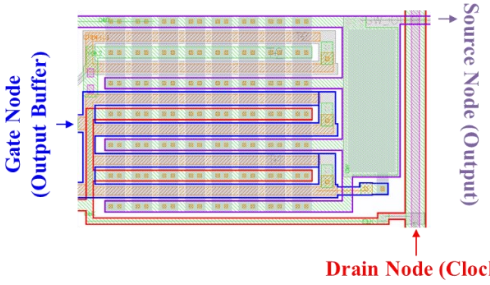

Figure 6. In the buffer TR, the clock line is connected to the drain node and forms a parasitic capacitance with the gate node.

The improved DA output waveform of the novel DA Scan Driver is applied as a margin that can downsize the buffer TR. The buffer TR size of the DA Scan Driver was downsized by 4 at a time based on Multiplier 32, and the output waveform was simulated. As a result, it was confirmed that t_f can be guaranteed even if multiplier value is applied at least 4 with Dual Path Discharge structure. However, even in 1H overlap operation, rising time of shorter than 1H is desirable to secure data charging time in pixel operation. From the simulation estimation of Fig.7, Half size of buffer TR (M=16) is selected and fabricated.

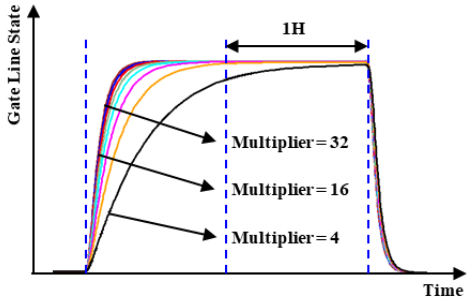

Figure 7. Simulation result of proposed circuit with various M of Buffer TR

3.3. 3-Terminal configuration Buffer TR

Due to the characteristics of the Dual Path Discharge circuit, power consumption can be reduced through down-sizing of the Buffer TR, and changes in the Buffer TR device configuration can be added. Currently, the Buffer TR of the oxide DA Scan Driver uses a four-terminal TR element by forming a top gate and bottom gate and gate syncing to improve ON current characteristics. In this case, similar to the multiplier value of the Buffer TR in Section 3.2, the ON current of the TR increases, which helps to improve the t_r and t_f of the output waveform, but increases the parasitic capacitance of the clock line connected by the drain node and the bottom gate. In this paper, it was confirmed that guaranteeing t_f even if the multiplier of the buffer TR is downsized to the half size through simulation and then formed into a three-terminal element by removing the bottom gate.

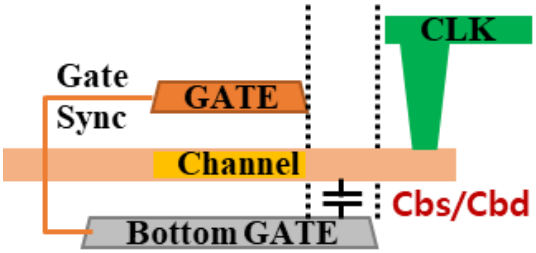

Figure 8. The bottom gate of the buffer TR, which consists of four terminals, forms a parasitic capacitance with a clock line that is a drain node.

3.4. Clock Line Position Optimization

In the current Top Emission display, a fan-out line for data voltage is formed at the bottom of the active area, and a scan driver for pixel driving is formed in the left-right dead space area. ELVSS line is formed outside the Scan Driver, and Pixel Metal is contacted at the top of the ELVSS line. In addition, the Cathode Metal, which is deposited on the front of the display, is contacted on the top of the Pixel Metal to complete the Anode to Cathode of the pixel structure.

When using this routing structure, the outer pixel metal of the scan driver is inevitably formed up to the upper part of the scan driver to reduce the cathode contact resistance, and parasitic capacitance with the clock line is formed. In this paper, the clock line of the Scan Driver is moved to the Active Area Side, and then the upper part of the clock line removes the pixel metal to form a structure that minimizes the parasitic capacitance between the clock line and the pixel metal for ELVSS contact. Pixel metal for ELVSS contact at the top of the clock line removed at the same time was used as clock line to apply triple line. Through this, the resistance of the clock line was reduced and applied to the t_f improvement of the output waveform.

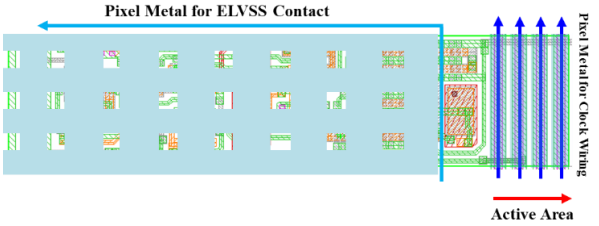

Figure 9. Change the clock line to the Active area side, remove the pixel metal for ELVSS contact at the top, and use it as a clock line.

4. Experimental Result & Conclusion

4.1. Novel DA Scan Driver TEG review and results

In order to evaluate the falling time improvement of output pulse, a Conventional DA Scan Driver was fabricated as a control group and a Novel DA Scan Driver with Dual Path Discharge and Carry Clock Less structure as an experimental group. By producing a real TEG consisting of 500 stages, the Buffer TR of the two circuits applied the same size when fabricating the TEG, and the RC load corresponding to the active line was applied. Test Points (TP) were applied to measure waveforms every 100 stages, and t_r and t_f evaluations were conducted for loads from 100 to 500 stages.

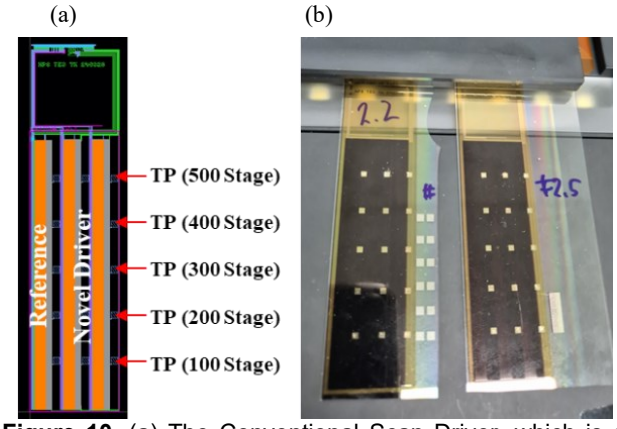

Figure 10. (a) The Conventional Scan Driver, which is a control group, and the Novel Scan Driver, which is an experimental group, were fabricated. (b) t_r and t_f for test points from 100 to 500 stages.

In the TP 500, where 100 layers of load were accumulated, the falling time of the novel DA Driver pulse was measured at an average of 301.9 ns for 16 samples, and the falling time of the conventional driver was measured at 374.7 ns, confirming a 19.4 % improvement in t_f. In TP 100, where 500 layers of load are accumulated, the falling time of the novel DA driver is 305.9 ns and the conventional driver is 440.9 ns, an improvement of 30.6 %. Thanks to the Dual Path Discharge circuit, the novel DA scan driver increased the falling time by only 4 ns compared to the 100-stage Output even in the 500-stage Output where the clock load increased, but the conventional DA Scan Driver where the clock load directly affects the falling time increased by 66.2 ns. Based on the actual measurement results, it was expected that the novel DA Scan Driver would be 57.2 % improved t_f when assuming 2300-stage display through linear interpolation.

Table 1. Evaluation result of Falling Time per Test Point of TEG

Test Point	Falling Time [ns]		Difference [ns]
	Conventional Scan Driver	Novel Scan Driver	
100	440.9	305.9	135.0
200	429.7	305.3	124.4
300	407.5	302.2	105.3
400	386.3	302.5	83.8
500	374.7	301.9	72.8

4.2. Power consumption simulation results

In order to confirm the power consumption improvement effect based on the novel DA Scan Driver mentioned in Chapter 3, power consumption simulation was performed. A total of 4 structures including Carry Clock removal structure, Buffer TR down-sizing and 3-terminalization, and Clock line position optimization were sequentially applied and evaluated. For the first, novel circuit that removed only the Carry Clock, the parasitic capacitance of the DA Clock Line was predicted to be 9.71 pF based on a 100-stage load and the power consumption was predicted to be 62.3 % then conventional. Second, when Buffer TR was downsized to half size, the parasitic capacitance of clock line was predicted to be 7.34 pF and power consumption was predicted to be 48.7 %. Third, when applying the 3-terminal structure that removed the bottom gate of the Buffer TR, the parasitic capacitance of the clock line was predicted to be 5.79 pF and the power consumption was 39.9%. Finally, when applying clock line position optimization and pixel metal structure change, the parasitic capacitance of clock line is 4.11 pF and power consumption is expected to consume 30.3 %. The DA Scan Driver power consumption of the conventional device, which uses the existing circuit and structure selected as the control group, is 100 % and is expected to improve by up to 69.7 % when all of the novel circuits and structures mentioned in this paper are applied.

Table 2. Simulation Results of Elements for Power Consumption Reduction at Each Stage

Type	CLK Parasitic Capacitance [pF]	Power Consumption [%]
Conventional Circuit	-	100
Novel Circuit	9.71	62.3
Buffer TR Down Sizing	7.34	48.7
3-Terminal Buffer TR	5.79	39.9
Clock Position Optimization	4.11	30.3

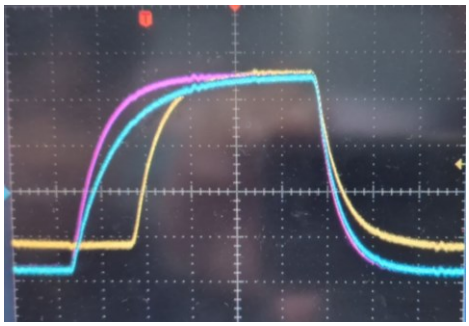

Figure 11. Waveform of fabricated TEG. Yellow is Conventional circuit, Pink is 3 Terminal Buffer TR and Cyan is structure containing all elements.

5. References

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