High-Reliability LTPS-TFT with Super-Low Gate Resistivity

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Abstract

This study explores the adoption of low-resistance gate wiring metals to enhance the scalability and functionality of LTPS-TFT displays. By using aluminum (Al) as the gate metal material, we were able to reduce the resistivity of about 1/5 of the conventional level. The reliability of LTPS-TFTs was significantly enhanced by incorporating a well-designed light-shield layer.

Author Keywords

LTPS-TFT; low resistivity gate metal; aluminum gate; high reliability; increasing in display size; high frequency driving

1. Introduction

Low-temperature polycrystalline silicon (LTPS) offers significantly higher mobility compared to amorphous silicon (a-Si) and oxide semiconductors, making it ideal for high-speed operation and enabling narrower display frames [1]. Consequently, LTPS-TFTs are widely used as switching devices in small- and medium-sized displays, such as those used in smartphones, notebook PCs, and automotive displays.

The fabrication of LTPS-TFT backplanes, typically requires high-temperature annealing to achieve favorable TFT characteristics. Therefore, heat-resistance metals like molybdenum (Mo) or molybdenum tungsten alloy (MoW) are commonly used as gate metal for LTPS-TFT. However, Mo and MoW have higher resistivity than aluminum (Al) and copper (Cu). The gate metal layer is often used for wiring patterns of peripheral circuits in addition to the display area. If the resistivity of the gate metal layer is high, the voltage drop in display areas and peripheral circuit areas will be large. So, it is necessary to set the panel drive voltage higher and to increase the thickness and width of the gate metal layer for panel driving.

Nevertheless, these issues become more critical as panel sizes grow and higher-frequency operation becomes standard, ultimately limiting the achievable panel performance.

To address these limitations, it is desirable to explore gate metal materials with lower resistivity than Mo and MoW in order to increase the size and functionality of LTPS-TFT panels. As for efforts to lower the resistivity of gate metal materials, studies of metal materials with high heat resistance have been reported [2,3].

In this paper, we fabricated LTPS-TFTs using Al as the gate metal material due to its lower resistance than Mo and MoW, low-cost, and compatibility with large-scale production, despite its relatively lower heat resistance. The TFT characteristics, gate metal resistance after the fabrication process, and Si crystallinity were evaluated. The effect of light shield (LS) layer and its shape dependence were also examined to improve the reliability of LTPS-TFTs. In addition, we fabricated LCDs by using LTPS-TFTs with an aluminum gate.

2. Fabrication of LTPS-TFT with aluminum gate

The panel backplane comprising LTPS-TFTs with an aluminum (Al) gate was fabricated on the glass substrate. To utilize Al as a gate metal material, it was necessary to develop a customized fabrication process to address the unique challenges associated with Al such as its lower melting point and distinct chemical resistance compared to conventional materials like molybdenum (Mo) and molybdenum-tungsten (MoW). The resistivity of the gate metal layer was evaluated after completing the backplane fabrication process for two cases: 1. using MoW as the conventional gate material and 2. Al as the low-resistance alternative. Resistivity measurements were performed by fabricating multiple thin-film patterns with thicknesses of 300 ~ 310 nm.

Figure 1 shows a probability plot comparing the resistivity distribution of the two gate metal layers. The results show that resistivity of the Al gate metal layer is ~ 1/5 of that of the conventional MoW layer. This demonstrates that the resistivity of the gate metal layer can be significantly reduced by using Al as the gate metal layer in our fabrication process.

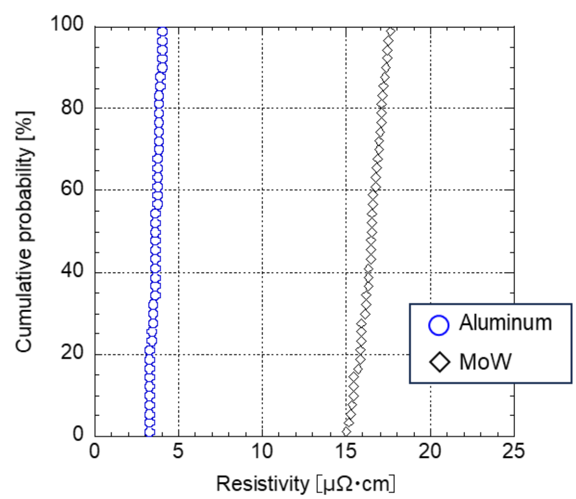

Figure 1. The resistivity of the gate metal layer using Al and MoW.

Next, we discuss the crystallinity of silicon (Si) in LTPS-TFTs following the TFT fabrication process. Figure 2 presents the results of electron backscatter diffraction (EBSD) analysis results for the Si regions of LTPS-TFTs fabricated by conventional MoW gate process and the proposed Al gate process. The analysis indicates that the grain size of crystalline Si is ~ 0.3 μm in both types TFTs, with no significant difference in the crystallinity

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between the intrinsic and doped regions. Notable, in the Al gate process, the doped region retains the same level of crystallinity as the intrinsic region after TFT fabrication process, comparable to the crystallinity achieved with the conventional MoW gate process.

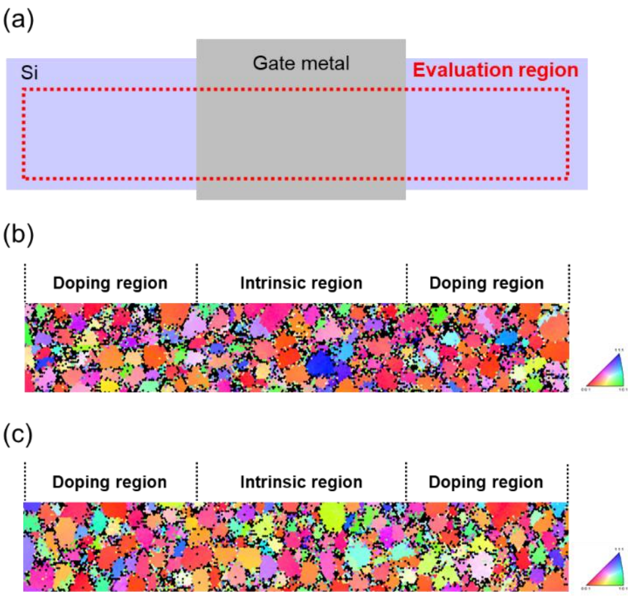

Figure 2. Evaluation of crystallinity of Si in LTPS-TFTs using EBSD analysis. (a) Schematic diagram showing the top view of LTPS-TFTs and evaluation region. Inverse pole figure maps of Si regions for LTPS-TFT (b) fabricated by the conventional MoW gate process and (c) fabricated by the Al gate process.

We evaluated the electrical characteristics of LTPS-TFTs fabricated using the conventional MoW gate process and Al gate process, focusing on their switching performance. In order to obtain excellent TFT characteristics, it is necessary to control the interface between the gate metal and gate insulator with fewer defects. In this study, we introduced barrier metal layer into the interface between Al gate electrode (GE) and gate insulator (GI) in LTPS-TFTs as shown in Fig. 3. This additional layer serves to optimize the interface, reducing potential defects and improving device reliability. The fabricated TFTs had a single-gate structure with a channel length and width of 8.0 μm and 10.0 μm, respectively and the impact of the barrier layer was evaluated.

Figure 4 shows the I_d-V_g characteristics of each fabricated TFTs. The TFTs fabricated by the Al gate process showed enhancement-mode characteristics, irrespective of whether a barrier metal layer was included. In addition, when compared with the TFTs fabricated by the conventional process with MoW gate, the same level of threshold characteristics and ON current values were obtained. This shows that the Al gate process can produce TFTs with favorable switching characteristics equivalent to those of the conventional process. Additionally, TFTs with a barrier metal layer showed an increase in ON current and a 1.1-fold increase in mobility compared to those without a barrier metal layer under the same fabrication conditions. These results indicate that inserting a barrier metal layer improves the characteristics of LTPS-TFT with Al gate metal.

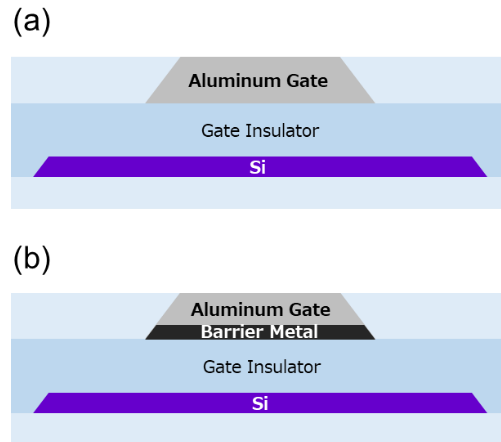

Figure 3. Cross-sectional schematic illustrations of (a) LTPS-TFT without a barrier metal and (b) that with a barrier metal between aluminum gate electrode and gate insulator.

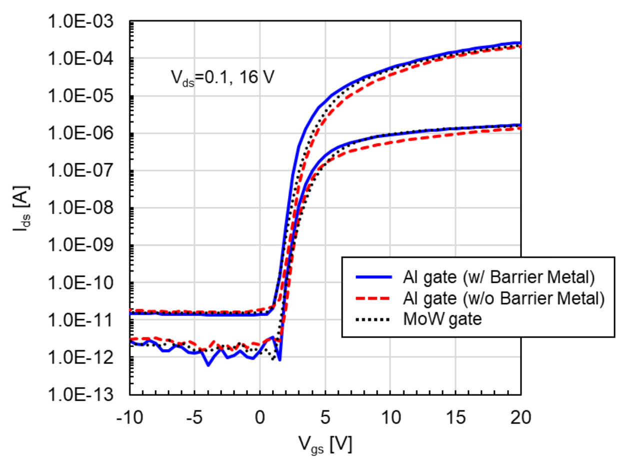

Figure 4. I_d-V_g characteristics of n-type TFTs fabricated by the Al gate process (w/ and w/o barrier metal) and the conventional process with MoW gate metal.

Next, we will discuss the impact of incorporating a barrier metal layer. When no barrier metal layer is present, it is possible that Al from the GE diffuses into the GI during the fabrication process, potentially creating new defect levels near the GE/GI interface. In contrast, when a barrier metal layer was inserted, the diffusion of Al into the GI was suppressed, and as a result, the interface state between GE and the GI being maintained in favorable condition through the TFT fabrication process. It is believed that this effect at the GE/GI interface improved the mobility compared to the case when a barrier metal layer was not inserted.

3. Improvement of reliability using LS layer and fabrication of LCDs

Next, we discuss the relationship between the mobility of LTPS-TFTs and the rate of current degradation observed during a stress current degradation test. We fabricated TFTs with various mobilities by changing the process conditions, and evaluated the rate of change in drain current before and after stress current application. The stress current was applied under the conditions specified in Table 1.

Table 1. Applied voltage conditions under stress current degradation test

Drain Voltage [V]	23.0
Gate Voltage [V]	Threshold voltage + 2.0
Stress time [sec]	4.0

The drain current degradation rate was calculated by measuring the drain current before and after the stress test, with V_{ds} of 0.1 V and V_{gs} of 23 V. This test was conducted using a double-connected TFT structure with a channel length of 3.5 µm and channel width of 10.0 µm. The results, shown in Fig. 5, reveal that the drain current degradation rate tends to increase in TFTs with higher mobility. This is likely due to the fact that higher the mobility leads to larger stress current being applied, intensifying the effects of hot carriers. While higher mobility is advantageous for achieving smaller TFT sizes, which supports narrow-frame displays, it also increases susceptibility to current degradation under stress. This creates a trade-off between mobility and reliability, as shown in Fig. 5. Achieving both high mobility and high reliability in the backplane fabrication process remains a hurdle due to this inherent trade-off.

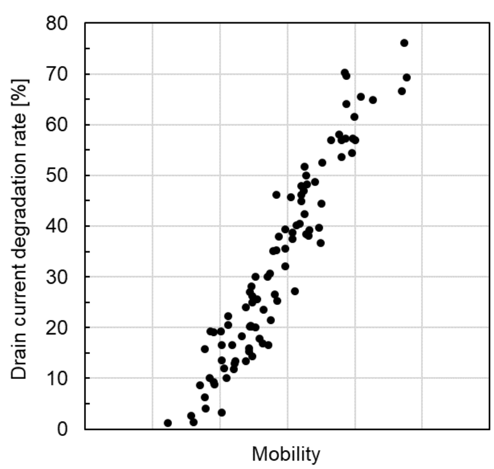

Figure 5. The relationship between the mobility of LTPS-TFTs and the current degradation rate.

To address these issues, we investigated the effect of incorporating light shielding (LS) layer beneath the LTPS-TFTs on device reliability. We fabricated TFTs with the same channel length width, but with and without the LS layer, and evaluated the current degradation rate in the stress current test. The results, shown in Fig. 6, reveal a significant difference in performance. For TFTs without LS layer, the current degradation rate increases with stress application time. On the other hand, TFTs with LS layer, the current degradation rate is suppressed, maintaining a low degradation rate even under extended stress conditions. These findings indicate that the insertion of the LS layer can suppress the current degradation during stress current tests, enhancing the device reliability.

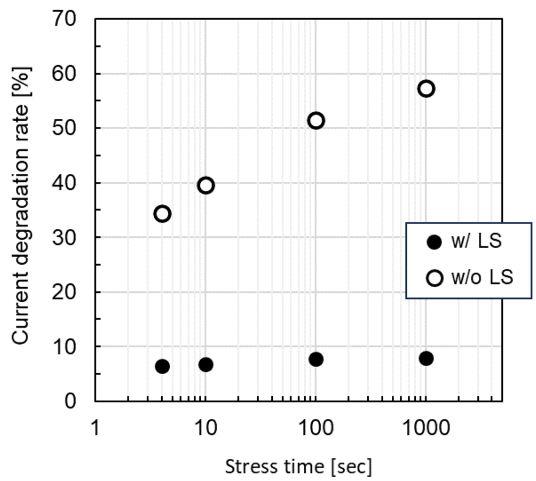

Figure 6. The relationship between the stress application time and the current degradation rate.

To further evaluate the impact of the LS layer on reliability improvement, TFTs were fabricated with different overlapping lengths between LS layer and the low-resistance area (LDD doping area), as shown in Fig. 7. The relationship between the overlapping length and the reliability of TFTs was analyzed. Figure 8 presents the relationship between the LS layer's overlap with the doping region and the lifetime of the current stress degradation test. In this study, the lifetime is defined as the time until the current degradation rate reaches 10% after the stress current is applied. The stress conditions for evaluating the current degradation rate are presented in Table 1.

The results indicate a substantial increase in lifetime as the overlapping length between LS layer and the doping region increased. Notably, when the overlapping amount was negative (i.e. part of the channel region did not overlap with the LS layer), there was no significant improvement in the lifetime. These results highlight the importance of ensuring a sufficiently large overlap between the LS layer and the doping region in order to improve the reliability of the LTPS-TFTs.

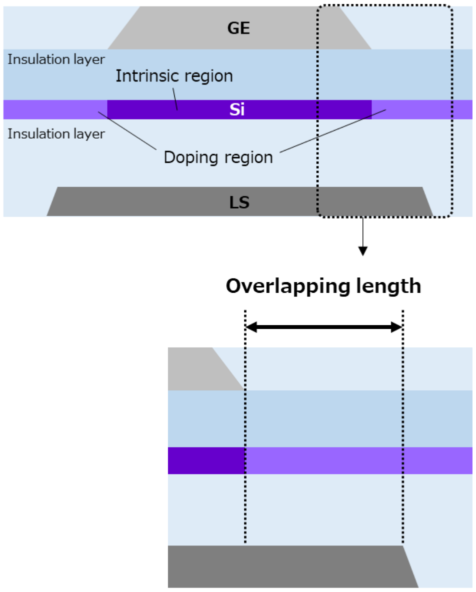

Figure 7. Cross-sectional schematic illustrations showing the overlapping length between the LS layer and the doping region in LTPS-TFTs.

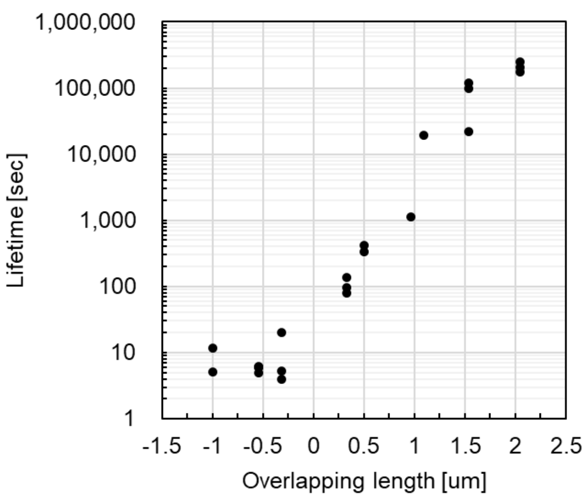

Figure 8. The relationship between the overlapping length of the LS layer and the doping region and the lifetime of LPTS-TFTs in the stress current degradation test.

Finally, we fabricated 16-inch LCDs by using LTPS-TFTs with Al gate. The Display image is shown in Fig. 9.

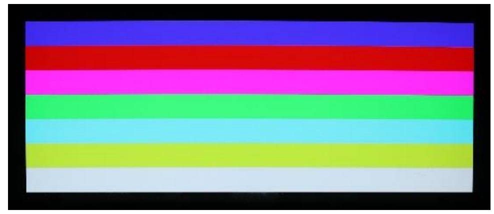

Figure 9. The image of the 16-inch LCD by using LTPS-TFTs with Al gate.

4. Conclusion

In this paper, LTPS-TFTs with Al gate metal were fabricated to reduce the resistance of the gate metal layer. The results demonstrated that the customized Al gate process successfully achieved a low-resistance gate metal layer while maintaining favorable LTPS-TFT characteristics with high-quality LTPS crystallinity, leading to realize LCDs with Al gate. Regarding TFT performance and reliability, the inclusion of a barrier metal layer between the Al gate electrode and the gate insulator improved the TFT mobility. The inserting of the LS layer overlapped with the doping region effectively suppressed current degradation and significantly improved reliability. The low resistance of the gate electrode layer enables the reduction of the driver chips combined with DeMux technology, potentially reducing costs. We believe that the Al gate process and the findings of this study will play a crucial role in enabling larger, higher performance, and less expensive LTPS-TFT displays.

5. References

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