Low-Power, Programmable Emission Control Driver Using Oxide Thin-Film Transistors Operating in Depletion Mode

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Abstract
This paper proposes a low-power, programmable emission control driver using amorphous indium-gallium-zinc-oxide thin-film transistors (a-IGZO TFTs) operating in depletion mode. To address the high-power consumption in oxide TFT circuits, it is proposed to minimize shoot-through current paths and not to adopt the series-connected two-transistor (STT) structure. The programmable emission control signal is generated by adjusting the start pulse, enabling pulse width modulation (PWM) operation for active-matrix organic light emitting diode (AMOLED) brightness control. Simulation results demonstrate stable operation and low-power consumption across a threshold voltage (V_{TH}) variation range from –2V to +2V, achieving up to a 66.0% reduction in power consumption compared to a prior study.

Author Keywords
Active-matrix organic light emitting diode (AMOLED); depletion mode; pulse width modulation (PWM); amorphous indium-gallium-zinc-oxide thin-film transistor (a-IGZO TFT); emission control driver

1. Introduction
With the growth of the smartphone and tablet PC markets, research has continued to develop thinner and higher performance displays. To achieve this, studies have focused on implementing slim bezels by integrating gate driver integrated circuits (ICs) into the panel instead of using external gate driver ICs. The gate drivers of conventional small-sized active-matrix organic light emitting diode (AMOLED) displays have used low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) with high mobility. However, the laser annealing process is expensive, and its application to larger substrates is challenging, which make it difficult to manufacture medium and large-sized displays economically [1, 2].

To overcome the limitations of LTPS, extensive research has been conducted on oxide TFTs, which have relatively high mobility, extremely low leakage current, and excellent uniformity. However, oxide TFTs operate in depletion mode, which negatively affects circuit behavior, and thermal and electrical bias stresses shift threshold voltage (V_{TH}) [3]. Therefore, we must carefully design oxide TFT gate drivers to operate without degradation in both depletion and enhancement modes.

To simplify processes and reduce production costs, research has been conducted on designing pixel circuits using only oxide TFTs. Pixel circuits need to compensate for V_{TH} variation of the driving TFTs. Therefore, an emission control driver needs to block current flows through OLEDs during compensation and to enable OLEDs to emit light after compensation [4]. Additionally, the emission control signal must support pulse width modulation (PWM) to globally adjust the brightness of the display panel [5]. Hence, the emission control driver must feature internal compensation and PWM operation by adjusting the pulse width of the output signal.

Conventional scan driver circuits typically utilize an inverter with a diode-connected structure, which can lead to significant power consumption due to static current through the inverter [6, 7]. In depletion mode, the current through the inverter increases dramatically, resulting in even higher power consumption. However, in conventional scan drivers, static current through the inverter flows in a short time, such as one or two line times, which does not significantly affect overall power consumption. In contrast, emission control drivers must generate output waveforms for most of a frame time except during the internal compensation period of the pixel circuit, resulting in prolonged inverter operation. Consequently, minimizing the current through the inverter is crucial for low-power emission control drivers.

This paper proposes a low-power programmable emission control driver operating in depletion mode. The proposed circuit generates a programmable emission control signal by simply adjusting the width of the start pulse. To minimize power consumption, the circuit utilizes a capacitor within the inverter to reduce the static current. Furthermore, the inverter, which does not employ a series connected two-transistor (STT) structure, reduces the required number of TFTs and ensures stable output waveform generation without increasing power consumption. The proposed circuit is validated through Smart-Spice simulations, demonstrating stable and low-power operation.

2. Proposed emission driver circuit

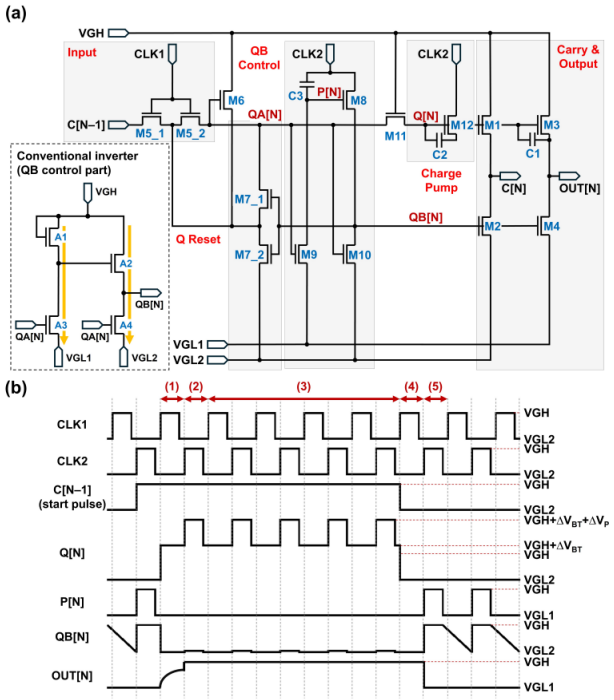

Fig. 1. (a) Schematic and (b) timing diagrams for the proposed emission control driver

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Fig. 1(a) illustrates the proposed circuit, which consists of 14 TFTs and 3 capacitors. The circuit can be divided into input part, Q reset part, QB control part, charge pump part, carry part, and output part. The input and Q reset parts employ an STT structure using M6 to prevent a voltage drop at the Q[N] node in depletion mode. The QB control part, a key feature of the proposed circuit, is composed of only 3 TFTs and 1 capacitor. P[N] node of the proposed QB control part becomes stably VGL1 due to no static current when QA[N] is high, which results in the very small V_{GS} of M8. Furthermore, since QA[N] is high, M10 remains fully turned on, ensuring stable QB[N]. The charge pump part bootstraps Q[N] node at high voltages through M12 and C2. Lastly, the carry and output parts are constructed using M1-M4 and C1. Fig. 1(b) shows the timing diagram corresponding to the generation of output waveforms over 11 line times by the proposed circuit. The pulse width of the output can be adjusted by modifying the width of the start pulse. A pair of non-overlapping clock signals with a low voltage value of VGL2 is employed, where the phases of the clock signals are opposite to each other. If CLK1 is connected to the stage N, CLK2 is connected to the stage N+1 in an alternating manner. The proposed circuit operates in five separate phases.

(1) Q Charging

When C[N–1] (or start pulse) signal is high and CLK1 transits to VGH, the voltage at Q[N] node rises to a high level through M5_1, M5_2 and M11, which turns on the pull-up TFT, M3, causing OUT[N] voltage to rise. At this point, the bootstrap effect in M3 and C1 causes Q[N] voltage to rise above VGH, increasing to $VGH+\Delta V_{BT}$. In depletion mode, although the bootstrap effect of C1 is present, V_{GS} of M5_1 remains 0 V, causing Q[N] to eventually drop to VGH. Meanwhile, due to the load on the gate line during this phase, OUT[N] rises slowly and does not fully reach VGH.

(2) Q Pumping

When CLK1 transits to VGL2, Q[N] node is left in a floating state. Subsequently, when CLK2 transits to VGH, Q[N] voltage is bootstrapped through M12 and C2, rising to $VGH+\Delta V_{BT}+\Delta V_P$ (in depletion mode, rising to $VGH+\Delta V_P$). OUT[N], which failed to reach VGH in Phase (1), rapidly rises to VGH due to bootstrapped Q[N].

(3) Emission

Immediately after phase (2), when CLK2 transits to VGL2, Q[N] node voltage decreases to $VGH+\Delta V_{BT}$ (in depletion mode, decreases to VGH) due to M12 and C2. Subsequently, CLK1 and CLK2 alternately rise and fall, maintaining Q[N] at a high voltage level, which ensures that OUT[N] remains stably at VGH.

(4) One Line Holding

When C[N–1] voltage drops to VGL2 and CLK1 goes to VGH, Q[N] voltage discharges to VGL2 through M11, M5_2, and M5_1. Since CLK2 goes to VGL2, P[N] voltage remains at VGL1, causing QB[N] voltage to also remain VGL2. Consequently, both Q[N] and QB[N] are at VGL2, keeping M3 and M4 in the off state. As a result, OUT[N] remains in a floating state, maintaining VGH for one line time.

(5) Pull Down

As CLK2 rises to VGH, P[N] increases to VGH due to C3. Simultaneously, QB[N] voltage rises through M8, turning M4 on, which causes OUT[N] to drop to VGL1.

The conventional inverter structure of Fig. 1(a) is used in gate drivers, where the diode-connected structure creates two current paths when QA[N] is high. First, when Q[N] is high, A3 is fully on, resulting in a significant static current from VGH to VGL1, thereby increasing power consumption. Second, the static current through A2 and A4 also contributes significantly to power consumption. Due to diode-connected A1, gate voltage of A2 is higher than VGL1. Consequently, V_{GS} of A2 is higher than VGL1 – VGL2, leading to substantial static current through A2 and A4, which further contributes to power consumption. This static current through A2 and A4 implies that QB[N] does not fully discharge to VGL2. Incomplete discharge of QB[N] further increases the static current through the pull-down TFT of the carry part under depletion mode, which leads to higher power consumption. As a result, the conventional inverter with a diode connection significantly increases power consumption due to these cascading effects, making it unsuitable for emission control drivers where Q[N] voltage remains high for extended periods.

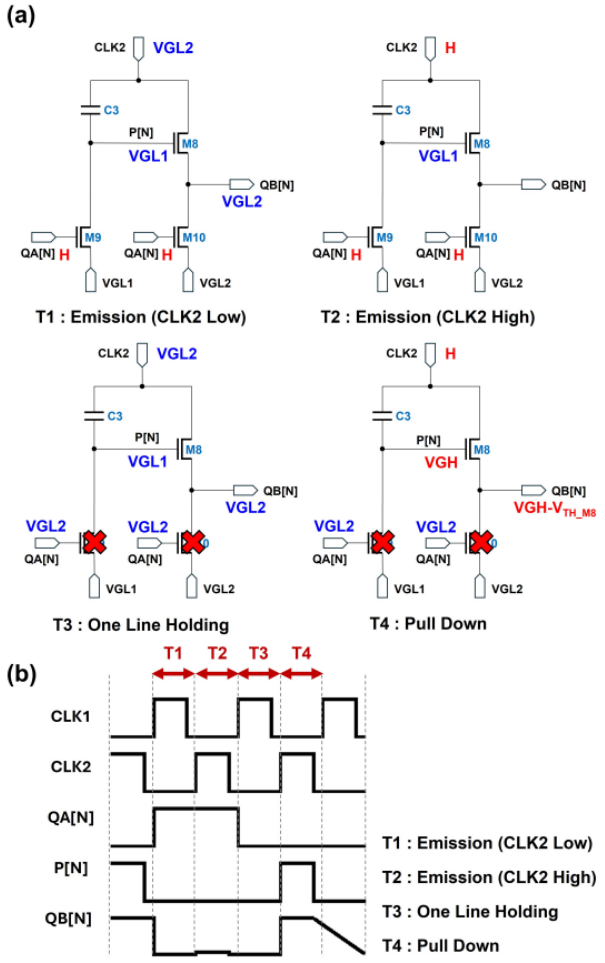

Fig. 2. (a) Schematic circuit diagram and operation sequence of the proposed emission control driver (b) Timing diagram of signal waveforms

Fig. 2(a) shows the proposed inverter circuit and its operation. Fig. 2(b) presents a timing diagram of signals divided into four phases to explain the operation. The reason the proposed circuit operates with low power consumption lies in its inverter structure.

During T1 (emission) phase, when QA[N] voltage is high and CLK2 voltage is VGL2, P[N] node voltage is maintained at VGL1 through M9. Unlike the conventional inverter utilizing a diode

connection, the proposed circuit prevents shoot-through current at P[N] node, resulting in lower power consumption and ensuring P[N] node is fully discharged to VGL1. Additionally, since CLK2 is at VGL2, no current flows through QB[N], which remains stably at the VGL2 voltage.

During T2 (emission) phase, when QA[N] is high and CLK2 goes to VGH, P[N] maintains VGL1 as M9 remains on. At this time, V_{GS} of M8, VGL1 – VGL2, creates a current path. However, limited current flows due to low V_{GS}. As a result, the small current flowing during T1 and T2, operating at a 40% duty cycle, significantly reduces power consumption compared to the conventional inverter.

T3 (one-line holding) is a crucial timing for the emission control driver to perform its shift register operation. During this phase, QA[N] voltage drops to VGL2, but CLK2 voltage also drops to VGL2, allowing P[N] voltage to remain stable at VGL1. As a result, M8 is slightly on, ensuring that QB[N] voltage is stably maintained at VGL2. Preventing QB[N] from rising is essential to avoid the discharge of floating OUT[N] voltage. The key feature of the proposed inverter circuit is its ability to stably maintain QB[N] at VGL2 voltage during T3 (one-line holding) phase.

T4 (pull-down) involves raising QB[N] to high, pulling down OUT[N] voltage. When CLK2 voltage rises to VGH, floating P[N] voltage is also raised to VGH through C3. Simultaneously, M8 is fully turned on, causing QB[N] voltage to rise. This demonstrates that the proposed inverter circuit not only enables low-power operation but also ensures stable operation as a shift register of the emission control driver.

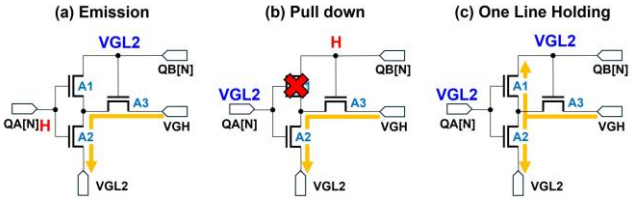

Fig. 3. Current path of STT structure during (a) Emission (b) Pull down (c) One line holding

The inverter of the proposed circuit has another advantage in that it does not utilize a STT structure. The STT structure not only increases the number of TFTs required for the driver but also causes continuous leakage current in depletion mode. As shown in Fig. 3(a), when QA[N] voltage is high, V_{GS} and V_{DS} of A3 are 0 V and VGH – VGL2, respectively, resulting in continuous leakage current. Similarly, as shown in Fig. 3(b), when QA[N] voltage is VGL2, V_{GS} of A2 is also 0 V, leading to sustained leakage current. The STT structure has a significant disadvantage in terms of power consumption.

Furthermore, the most critical drawback of the STT structure arises during the one line holding phase, which is essential for the emission control driver. As depicted in Fig. 3(c), QA[N] and QB[N] must maintain VGL2 to keep OUT[N] floating for the duration of one line time. In depletion mode, V_{GS} of A1 and A3 is 0 V, keeping them on, which causes QB[N] node voltage to charge. If QB[N] voltage exceeds the V_{TH} of the pull-down TFT (M4), OUT[N] voltage drops too early, creating a critical issue.

While the STT structure is effective for maintaining high voltage, it is critically ineffective in maintaining low voltage. Since the proposed circuit does not employ the STT structure, it can stably maintain QB[N] voltage at VGL2 during one line holding phase.

3. Simulation Results

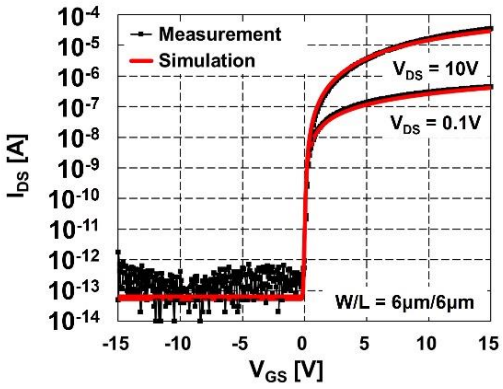

Fig. 4. Transfer curve of n-type a-IGZO TFT

The proposed emission control driver was simulated based on fabricated n-type a-IGZO TFTs. Fig. 4 illustrates the measured and modeled transfer curves of the a-IGZO TFT used in the circuit, with a channel width of 6 μm and a channel length of 6 μm. The a-IGZO TFT exhibits a V_{TH} of 0.005 V, a subthreshold swing (SS) of 210 mV/dec, and a field-effect mobility (μ) of 8.9 cm²/V·s. The voltage levels for VGH, VGL1, and VGL2 were set to 15 V, –5 V, and –8 V, respectively, with CLK1 and CLK2 signals having voltage swings between VGH and VGL2 with a 40% duty cycle. The capacitive and resistive loads were assumed to be 120 pF and 15 kΩ, respectively. The target resolution and frame rate were set at 3840 × 2160 and 60 Hz. A line time of 8 μs and a vertical blank length of 10 line-times were set. The simulation was conducted with two identical emission control drivers operating simultaneously from both ends, and the output waveform was analyzed at the midpoint of the gate signal line, representing the worst-case condition.

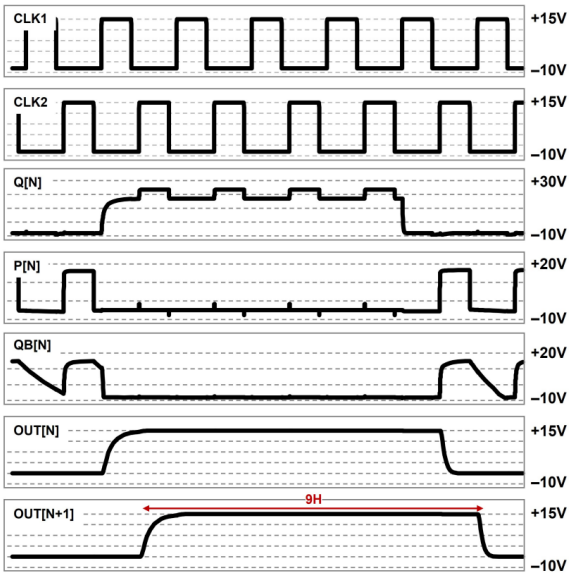

Fig. 5. Simulated waveforms for 9-line-time pulse width output

Fig. 5 illustrates the simulation results of the proposed emission control driver, showing the voltages at each node and the output waveform for 9-line-time pulse width. During the generation of the output waveform, Q[N] consistently maintains a stable high voltage and pumped high voltage, while QB[N] remains stably close to the

VGL2 voltage. The output waveform also demonstrates a stable output at the VGH voltage.

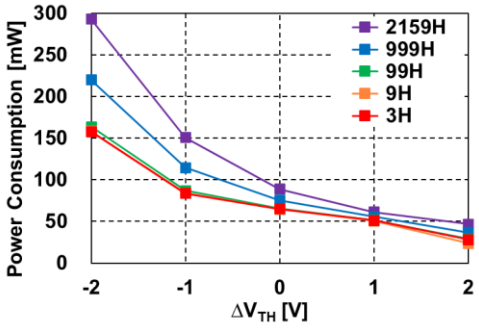

Fig. 6. Power consumption of emission control driver depending on V_{TH} and output pulse width

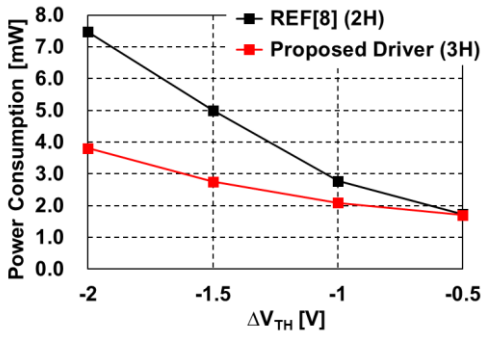

Fig. 7. Power consumption depending on V_{TH} of proposed emission control driver compared with the previous study [8]

Fig. 6 presents the power consumption of the output waveform with varying pulse widths across 2,160 stages under different V_{TH} variations. When generating an output waveform with the maximum pulse width of 2,159H, the power consumption reaches a peak of 292.9 mW at ΔV_{TH} = –2 V. Fig. 7 illustrates a comparison of the power consumption between the proposed circuit and a previously reported emission control driver that utilizes a diode-connected inverter based on oxide TFTs operating in depletion mode [8]. The comparison was conducted under identical conditions, including gate line loads (10 kΩ resistance, 150 pF capacitance), 50 stages, 1,080 vertical lines (FHD resolution). While the previously studied emission driver generated an output waveform with a pulse width of 2-line times, the proposed driver was evaluated under a 3-line time pulse width condition. The power consumption caused by the clock line load was excluded from the analysis. In general, emission control drivers can only generate output waveforms corresponding to either even or odd line times, making direct comparisons under identical output conditions challenging [9]. However, even under the condition where the proposed circuit extends the output waveform duration by 1 additional line time compared to the previous studied driver, it still achieves a 49.1% reduction in power consumption in depletion mode (ΔV_{TH} = –2 V), confirming its capability for low-power operation.

4. Conclusion

This paper demonstrates a low-power emission control driver based on a-IGZO TFTs capable of operating in depletion mode. The proposed circuit stably generates programmable output waveforms under both depletion mode and enhancement mode conditions. The inverter in the proposed circuit forms only a single current path and eliminates the need for an STT structure, reducing the number of TFTs required for circuit design and overall power consumption. Additionally, during one line holding phase, the circuit maintains QB[N] node at a low voltage, ensuring stable output waveform generation. Simulation results indicate that the power consumption of 2,160 stages is only 292.9 mW, representing a 66.0% reduction compared to the previously studied emission control driver. The proposed circuit has been successfully validated featuring low power consumption and PWM driving support, even under the depletion mode condition.

5. Acknowledgements

The EDA tool was supported by the IC Design Education Center (IDEC), Daejon, South Korea. This work was supported by Samsung Display Co., Ltd.

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