Research on the Causes of OLED White Spot Defects and Exploration of Improvement Directions

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Abstract

With the development of OLED display technology and the intensification of competition in the OLED mobile phone product market, consumers have increasingly high requirements for the display quality of OLED mobile phones. Higher product quality and yield requirements encourage panel manufacturers to enhance their competitiveness through equipment improvement, process improvement, and product design optimization. Poor white spots are an important factor affecting display quality. This article studies the mechanism of white spot defects and provides an effective direction for improving particles, optimizing equipment, and optimizing process parameters to reduce the impact of white spot defects.

Keywords

OLED; Particle; Activation; White Spot

1. Introduction

White spot defect is a new type of defect in OLED products, occurring during the BP production process. Various factors contribute to the formation of white dot defects, but ultimately it is due to the local drive current being affected and deviating from the set value, which eventually causes local pixels to light up, as shown in Fig. 1. Since its occurrence, white dot defects have consistently ranked among the top three defects in BP, significantly impacting the yield and quality of OLED products. In this paper, we analysis how White Spot generated, and then propose methods to improve white spot.

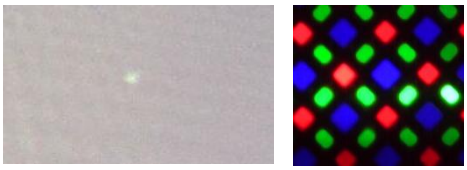

Figure 1. White spot light on

2. Analysis

By studying the phenomenon of white spot defects and process monitoring, we found that these defects occur in layers close to Poly-Silicon. Such process defects affect the V_{th} value of the Driver TFT of surrounding pixels, causing brightness abnormalities in multiple pixels.

2.1 Matching analysis of white spot and process defects

Through FIB analysis of numerous white spot cases, it was found that the defects causing white spots are mainly distributed in the Barrier/Multi/GI1/GI2 layers, adjacent to the Poly-Silicon layers, as shown in Fig. 2. These defects are primarily of two types: Type 1 involves a small defect causing a crack in the layer, and Type 2 involves larger contamination forming a void. Despite the defect itself being only a few dozen micrometers, it can affect several pixels (hundreds of micrometers), so we believe this anomaly is not an issue with the pixel where the defect is located, but rather that the defect affects the characteristics of the surrounding pixels。

2.2 V_{th} variation and electrical signal analysis in white spot areas

By using special sample preparation methods to test the Driver TFT in the display area, it was found that in the white spot abnormal area, the V_{th} value of the Driver TFT is negatively offset by about 1.1V compared to the OK area, as shown in Table 1.

Driver TFT △V_{th}		
Sample ID	White Point Area	OK Area
1	-1.11	Ref.
2	-1.12	
3	-1.08	
4	-1.07	
5	-1.13	
Average	-1.1	

Table 1. V_{th} Negative Offset

Signal debugging was performed on products with white spot defects, as shown in Fig. 3. In the first step, by adjusting the V_{int} and V_{data} signals to be consistent, the white spot abnormal area turns black. In the second step, by significantly negatively adjusting the V_{int} and V_{data} signals overall, the black area disappears. This indicates that the V_{th} of the Drive TFT (T3) is significantly negatively offset and that a higher Gate voltage is required to turn on the Drive TFT.

Thus, both practical measurements and circuit analysis confirm that the white spot defect is caused by a local negative offset in V_{th}.

2.3 Analysis of V_{th} Negative Offset Caused by Microscopic Defects

Defects within the layers can cause a negative offset in the V_{th} of the pixels around them through two main mechanisms. Mode 1 involves affecting V_{th} Doping, as shown in Fig. 4. During the V_{th} doping process, the defect forms a micro field with the defect at its core, causing the B^+ ions to deviate from their intended paths or blocking ion implantation at the Poly-Silicon surface, ultimately leading to reduced ion dosage in the defect and its surrounding area, thus causing the electron hole of PMOS TFT decreased, leading to V_{th} negative offset. Mode 2 affects activation, as shown in Fig. 5. During the activation process, defects encapsulated in dense SiN/SiO deform and expand under high temperatures (over 400 degrees Celsius), which can even break the inorganic film layer. The resulting voids allow H^+ ions to escape due to the concentration gradient, reducing the hydrogen content in the defect and its surrounding area, thus causing the electron hole of PMOS TFT decreased, leading to a V_{th} negative offset.

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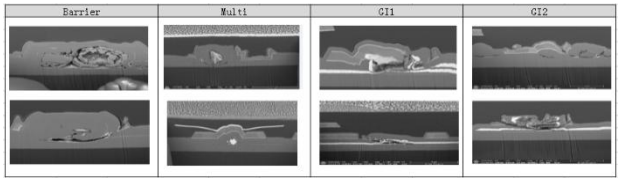

Figure 2. FIB of process defects

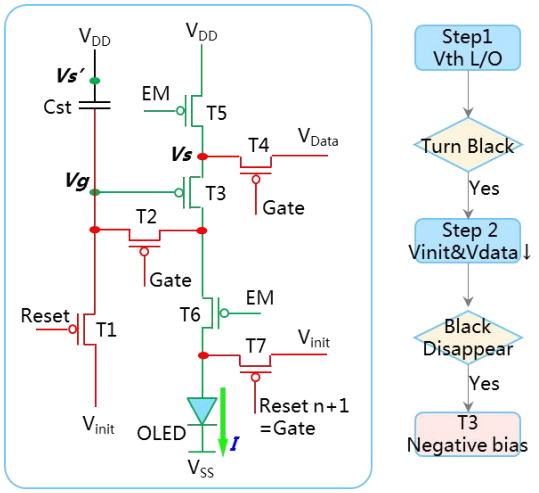

Figure 3. Analysis of 7T1C Circuit

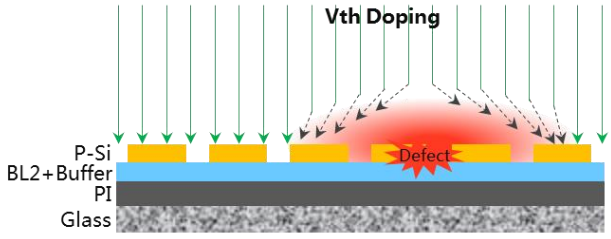

Figure 4. Mechanism of implant affecting white spot

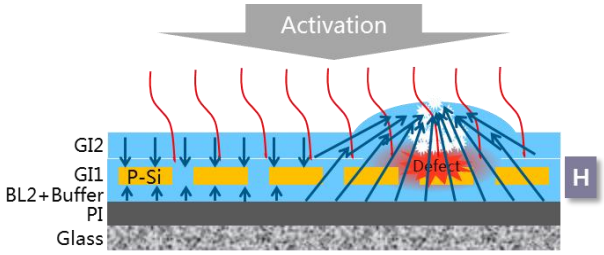

Figure 5. Mechanism of activation affecting white spot

2.4 White Spot caused by other reasons

According to the characteristics of PMOS TFT, when Vinit1 $V_{data}<V_{th}$, stages ① (initialization), ② (signal writing), and ③ (display) can be executed normally, completing T3 V_{th} compensation and signal writing, and displaying normally.

When T3 V_{th} continues to be negatively biased and V_{init1} $V_{data}>V_{th}$, stage ② signal cannot be written, and compensation & signal writing fails. If the Ids of stage T3 remains between I_{off} and I_{Vth} and cannot be turned off or turned on normally, a white spot will form, as shown in Fig.

6.

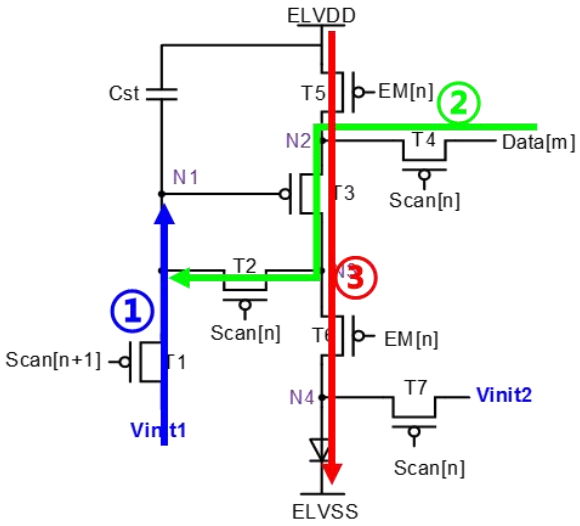

Figure 6. White spots causing by V_{th} negative bias

2.5 White Spot caused by other reasons

The causes of white spots are varied, and some process defects are invisible types, but these will not be studied in this paper.

3. Experiment

3.1 Improving white spots by enhancing cleaning capability

Through the previous microscopic analysis of defects causing white spots, it is concluded that they are mainly distributed in the inorganic layers from Barrier to GI2. Therefore, we propose four directions for removing particles in these layers. Split A: Enhance cleaning capability before Multi DEP to reduce particles before Multi DEP; Split B: Enhance cleaning capability before GI1/2 DEP to reduce particles before GI1/2 DEP; Split C: Enhance cleaning capability before doping to reduce particles that block injection; Split D: Enhance Gate1 strip capability to reduce particles from dirt adherence. Products are validated to the lighting judgment under these four conditions, with four G6 Glass pieces for each condition and an additional four pieces produced under mass production conditions for comparison.

3.2 Improve white spot by enhancing PECVD equipment and process

In addition to removing interface particles by enhancing cleaning capability, we also need to improve the internal particles in the PECVD layers. We propose six directions for verification. Split A: Change diffuser material to reduce particles from impurities precipitated in high-temperature processes; Split B: Optimize S/F material and configuration to reduce particle accumulation in equipment dead corners; Split C: Add plasma treatment before GI1/2 DEP to reduce particles from the film-forming process; Split D: Optimize clean season gases to enhance the film's particle adsorption capability. Products are validated to the lighting judgment under these four conditions, with four G6 Glass pieces for each condition and an additional four pieces produced under mass production conditions for comparison.

3.3 Improve white spot by optimizing ion implant

process

From the Mode 1 analysis model in section 2.3, we know that the ion implant process is a trigger for white spots. We propose two experimental conditions for the ion implant process. Split A: Perform ion implant after ELA to reduce the impact of defects produced after Multi on ion implant; Split B: Keep the ion implant site unchanged but increase the implant concentration to positively adjust the overall V_{th}. Products are validated to the lighting judgment under these two conditions, with four G6 Glass pieces for each condition and an additional four pieces produced under mass production conditions for comparison.

3.4 Improve white spot by optimizing activation process

From the Mode 2 analysis model in section 2.3, we know that the activation process is a trigger for white spots. We propose five experimental conditions for the activation process. Split A: Move activation forward so that defects expand early and are then covered by the GI layer to avoid H^+ leakage; Split B: Cover with multiple layers of inorganic film to reduce inorganic film cracking near Poly-Silicon and avoid H^+ leakage; Split C: Use a step-by-step activation process to avoid excessive energy in a single activation causing GI cracking and H^+ leakage. Four G6 Glass pieces are used for each condition, with an additional four pieces produced under mass production conditions for comparison.

4. Results and discussion

4.1 Result of the improvement by enhancing cleaning capability

The results show that improving certain cleaning capabilities can reduce the incidence of white spots. Data indicate that although Splits A/B/C can reduce process defects, they do not significantly contribute to decreasing the incidence of white spots. However, enhancing the Gate1 strip capability (Split D) and improving defects from dirt adherence can reduce the white spot incidence by 5.2% relative to mass production conditions, as shown in Table 2.

Optimization of Cleaning Capability			
Split	△Number of process defects	△White spot defect rate	Side Defect
A	-11%	-0.7%	None
B	-8%	0.6%	None
C	-21%	-0.7%	None
D	-11%	-5.2%	None
Remarks: 1. Relative value of mass production conditions			

Table 2. Result of enhancing cleaning capability

4.2 Result of the improvement by enhancing PECVD equipment and process

The results show that some cleaning capability improvements can reduce the incidence of white spots. Although Splits A/B/C/D can reduce process defects, Splits C/D do not significantly contribute to decreasing the white spot incidence. By improving PECVD equipment hardware, Splits A/B can reduce particles from precipitation and accumulation, leading to a 6.3% and 2.4% reduction in white spot incidence, respectively, relative to mass production conditions, as shown in Table 3.

Optimization of PECVD Equipment&Process			
Split	△Number of process defects	△White spot defect rate	Side Defect
A	-27%	-6.3%	None
B	-23%	-2.4%	None
C	-9%	-0.6%	None
D	-5%	-0.1%	None
Remarks: 1. Relative value of mass production conditions 2. Verify spilt A/B/C/D in four times			

Table 3. Result of enhancing PECVD equipment and process

4.3 Result of improvement by optimizing ion implant process

Adjusting the ion implant process can preferentially reduce the incidence of white spots, but it introduces side defects such as GM NG and ISFOM NG, as shown in Table 4. Therefore, from the current experimental results, research on the ion implant process is not yet ready for mass production and requires further exploration.

Optimization of Implantation Process		
Split	△White spot defect rate	Side Defect
A	-40.0%	GM NG
B	-12.7%	Isfom NG
Remarks: 1. Relative value of mass production conditions		

Table 4. Results of optimizing ion implant process

4.4 Result of improvement by optimizing activation Process

Optimizing the activation process can significantly reduce the incidence of white spots. However, simple adjustments such as moving the activation process (Splits A/B) can reduce white spot incidence but introduce significant side defects. The step-by-step activation process in Split C is more effective, reducing the incidence of white spots without causing side defects. However, the production capacity of activation equipment needs to be considered due to the step-by-step process.

Optimization of Implantation Process		
Split	△White spot defect rate	Side Defect
A	-72.0%	Point Defect Raising 132%
B	-41.3%	Line Defect Raising 18.8%
C	-85.6%	None
Remarks: 1. Relative value of mass production conditions		

Table 5. Results of optimizing activation process

5. Conclusions

This paper analyzes the influencing factors of White Spot and improves them by various methods. The influencing factors of white spot include Barrier to GI Particle, implant process, activation process, etc. After a series of tests, the improvement methods mentioned in this paper have varying degrees of improvement effects on white spot. It is of great guiding significance for improving low white spot in the OLED industry.

6. Acknowledgements

The authors gratefully thank the supports of Chengdu BOE Optoelectronic Technology Co., Ltd.

7. References

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