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4,032-PPI Vth Compensation Pixel Circuit for OLEDoS

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Abstract

In this paper, a 7T1C pixel circuit for 4,032-PPI is proposed. In order to implement organic light emitting diode-on silicon (OLEDoS) for high-resolution micro-display, pixels must be integrated in a small area. However, in the case of a small transistor, a driving transistor current deviation occurs due to Vth variation, and image quality is deteriorated. The proposed 7T1C pixel minimizes the current deviation of the driving transistor through the Vth compensation circuit. In addition, the source and body voltages of the driving transistor were the same so that there was no body effect of the CMOS circuit. In order to implement 4K resolution, verification was performed by designing the pixel layout in a 6.3um pixel pitch using an 8V transistor. As a result, the current deviation is improved from ±10.6% to ±2.75% when ±15mV Vth deviation of transistor is applied.

Author Keywords

OLEDoS; Micro Display; 4K; Vth Compensation; Body Effect

1. Introduction

Micro-displays are used as virtual reality (VR) and augmented reality (AR) applications. Among micro display technologies, organic light emitting diode-on-silicon (OLEDoS) has advantages in high contrast ratio, wide color area, and thin display. In particular, by using a silicon backplane-based micro process, pixels and driving circuits can be integrated into one chip, and are advantageous for high-resolution and high-speed driving. However, in order to implement high-resolution OLEDoS, pixels must be integrated in a small area. In the case of small transistors, Vth distribution increases, even though the same data voltage is applied, current deviation of each pixel occur. In addition, when a silicon-based transistor is used, a Vth compensation error is caused by a body effect if the source and body voltage of the driving transistor are changed after Vth compensation. [1-3] In order to solve this problem, this paper proposes a 7T1C pixel structure for 4,032 ppi OLEDoS that can compensate for Vth without body effect.

2. Proposed Pixel Circuits and Operation

Figure 1 is a proposed pixel 7T1C circuit diagram. The proposed pixel consists of one driving transistor, six switching transistors, and one capacitor. Each of the six switching transistors is driven by a gate driver, and a current is driven by varying a driving transistor gate voltage through a data signal. In the case of power, it consists of an ELVDD and an ELVSS voltage for OLED driving, VINT for Anode initialization, and a VPRE for initializing both ends of the capacitor. Figure 2 shows the operation of 7T1C pixel, and Figure 3 shows the timing diagram of 7T1C pixel.

$$Vb \ \& \ Vc = VPRE \ll EVLDD - |Vth| \text{ of T1} \quad (1)$$

$$Va = Vint + |Vth| \text{ of T5} \quad (2)$$

Figure 2. (a) represents an initialization operation and corresponds to the first and second phase of timing diagram in Figure 3. The voltages Vb and Vc at both ends of the capacitor are initialized to the VPRE voltage. (Equation 1) The voltage Va is also initialized to the VINT voltage. (Equation 2).

$$Va = Vint + |Vth| \text{ of T5}, Vb = Vdata, \quad (3)$$

$$Vc = EVLDD - |Vth| \text{ of T1} \quad (4)$$

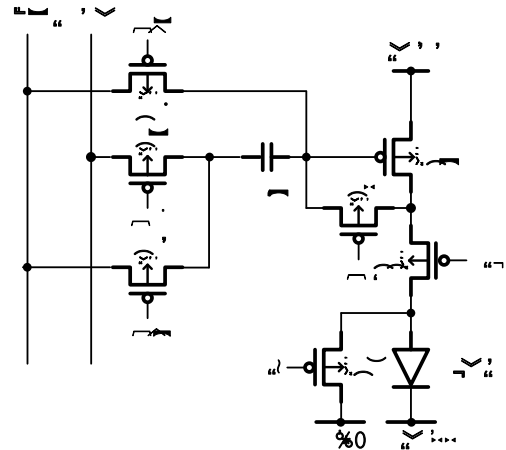


Figure 1. A Schematic of 7T1C Pixel Circuit

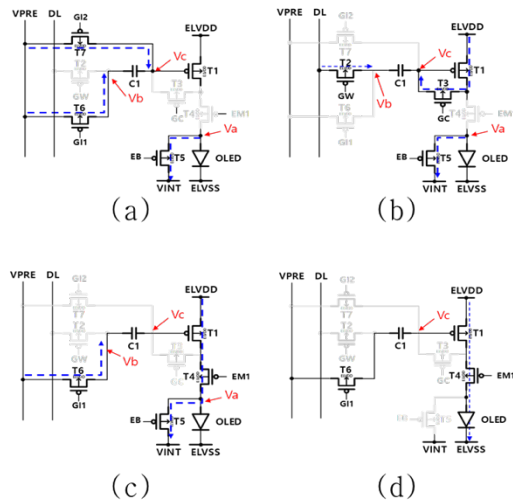


Figure 2. An Operation of 7T1C Pixel Circuit

Figure 2. (b) represents a Vth compensation operation and corresponds to the third phase of timing diagram in Figure 3. When the Va node is initialized to Vint+|Vth| voltage and the Vb node is applied to the data voltage (Equation 3), the T3 switch is turned on to store the ELVDD-Vth voltage in the Vc node. (Equation 4)

$$Vb = VPRE, Vc = EVLDD + VPRE - Vdata - |Vth| \quad (5)$$

$$Va = Vint + |Vth| \text{ of T5} \quad (6)$$

Figure 2. (c) represents a anode holding phase and corresponds to the fourth phase of timing diagram in Figure 3. As the Vb node changes from the data voltage to the VPRE voltage, the Vc node

adds the bootstrapped voltage to the previous V_{th} compensated voltage. (Equation 5) At this time, the V_a node is maintained at $V_{int} + |V_{th}|$ voltage to prevent the low gradation luminance from rising due to the parasitic capacitance charge of driving transistor drain voltage. (Equation 6)

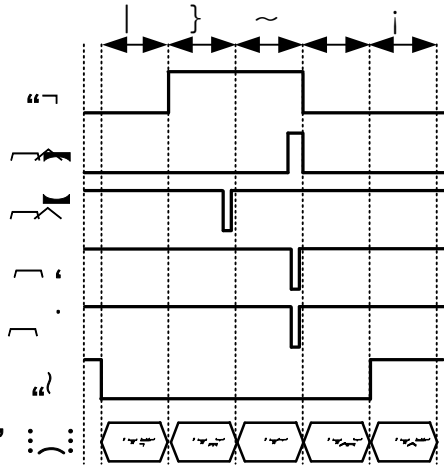


Figure 3. Timing Diagram of 7T1C Pixel Circuit

$$I_{OLED} = I_0 \times \exp\left[\frac{q(V_{sg} - |V_{th}|)}{Hkt}\right] \quad (7)$$

$$V_{sg} = ELVDD - V_c, \quad V_{sg} - |V_{th}| = V_{data} - VP_{RE}$$

Figure 2. (d) represents a OLED emission phase and corresponds to the fifth phase of timing diagram in Figure 3. As shown in Equation (7), V_{th} and $ELVDD$ terms are removed from the driving transistor Vsg during emission phase. As a result, the current deviation due to V_{th} and body effect is greatly improved.

Figure 5 is the standardized luminance based on the target luminance according to the data voltage. Based on the contrast ratio of 1,000,000:1, the data voltage range is 1.1 to 2.0V. Figure 6 shows the current deviation by gray level before and after V_{th} compensation when there is a V_{th} deviation, $\pm 15mV$. Based on the 11 gray, the uncompensated current deviation is $\pm 10.6\%$, and when the proposed V_{th} compensation is applied, the current deviation is $\pm 2.75\%$. Table 1 shows the SRU images measured for 255, 127 Gray. Figure 6 shows the image of the product with 7T1C pixels

3. Simulation Results

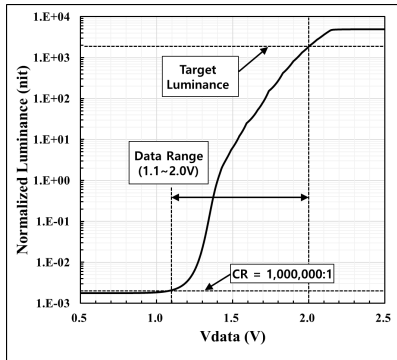


Figure 4. Data Swing Range of 7T1C Pixel Circuit

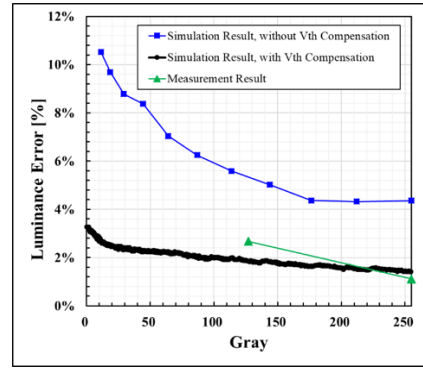


Figure 5. Simulation and Measurement result of Current Error with V_{th} compensation and without V_{th} compensation

	7T1C	255G	127G
With V_{th} Compensation			
SRU		98.9%	97.3%

Table 1. Measurement result of Short Range Uniformity (SRU)



Figure 6. 4032-PPI Image

4. Conclusion

In this paper, a 7T1C pixel circuit for 4,032 PPI OLEDoS was proposed. Through the V_{th} compensation circuit, TR V_{th} variation was compensated to improve the current deviation from $\pm 10.6\%$, to $\pm 2.75\%$.

5. References

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