Systematic Study on Scanning Direction of Excimer Laser Annealing in p-Type Low-Temperature Polycrystalline Silicon Thin-Film Transistors

Qian Xiao, Guoren Hu, Quanhu Yang, Guixue Zhang, Rui Zhang, Shirong Zhang, Haipeng Wang, Minyang Deng, Chunrong Lai , Yunzhi Wang, Wuyang Zhao

Mianyang BOE Optoelectronics Technology Co., Ltd.,
No. 198, Middle section of Kefa Avenue, High-Tech Zone, Mianyang, China

Abstract

The bright points caused by off-state leakage current constricted the reliability of LTPS TFT. The effect of ELA scanning direction on TFT properties was demonstrated. The trap state densities of grain boundary and poly-Si/SiO_2 interface and barrier were calculated to clarify the mechanism of high off-state leakage current.

Author Keywords

Low temperature poly-crystalline silicon (LTPS); Thin-film transistor (TFT); Off-state leakage current; Barrier

1. Introduction

Low-temperature poly-crystalline silicon thin film transistor (LTPS TFT) with the outstanding comprehensive performance which mobility higher than amorphous silicon and lower cost than mono-crystalline silicon is widely used in display manufacturing. The poly-crystalline silicon is consisted with numerous mono-crystalline silicons and the mono-crystalline is connected by highly disordered grain boundaries. Therefore, the poly-crystalline silicon with higher leakage current than mono-crystalline silicon and amorphous silicon due to the existence of grain boundary.

In the use of TFT, the panel with bright points induced by the off-state leakage current which affected the reliability of panel. The researches shown that the characteristics of TFT be affected by the height, number and position of the grain boundary [1-5]. Sequential lateral solidification (SLS) have been reported by many researches [6-8]. The results show that the parallel TFT with higher electron field effect mobility and higher leakage current than perpendicular TFT. The different scan direction of ELA on substrate in the manufacturing can result in the differences in the number and height of grain boundaries through which current passes in the TFT.

Therefor, it is necessary to study the different ELA scanning direction on substrate for the reliability of TFT in the application. In this work, the two TFTs with different crystal orientation were fabricated for clarified the effect on characteristic. Furthermore, the mechanism of different crystal directions on the off-state leakage current is elucidated.

2. Methods

Conventional top-gate p-channel LTPS TFTs were prepared on polyimide substrate for experimental. Firstly, a polyimide was coated onto a glass substrate. Subsequently, a barrier layer composed of SiN_x and SiO_x was deposited through the process of plasma-enhanced chemical vapor deposition (PECVD). Then, an amorphous silicon (a-Si) layer was deposited onto the buffer layer using PECVD, which was subsequently crystallized by excimer laser annealing (ELA). Following this, a SiO_x layer was deposited as the gate insulator (GI) via PECVD, and molybdenum (Mo) was deposited as the gate electrode through physical vapor deposition (PVD). Fig. 1 shows the schematic cross-sectional view of the fabricated LTPS TFTs. The TFT with current direction perpendicular to the ELA scanning direction is shown in Fig. 1 (a). And the TFT with current direction parallel with the ELA scanning direction is shown in Fig. 1 (b).

The TFT field effect mobility (μ_{FE}) was obtained from the transconductance ($\partial I_D/\partial V_G$), where I_D is the drain current and V_G represents gate bias. The threshold voltage (V_{TH}) was obtained from W/L*I as I=1.0E-8 A. The subthreshold swing, SS was taken as $(\partial \mathrm{Log} I_D/\partial V_G)^{-1}$ over the range of 1.0E-10 A $\leq I_D \leq$ 1.0E-9 A, with V_D = −5.1 V. The channel width (W) and channel length (L) of the measured TFTs were both 2 μm and 5 μm, respectively.

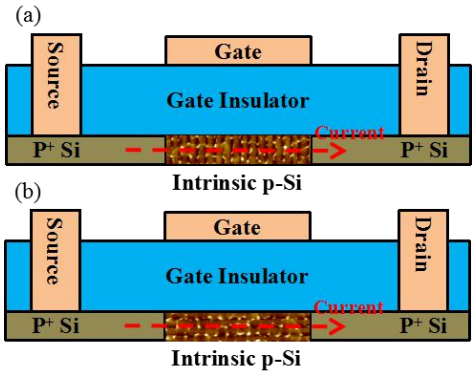

Figure 1. The schematic cross-sectional view of the fabricated LTPS TFTs on glass: (a) the TFT with current direction perpendicular to the ELA scanning direction; (b) the TFT with current direction parallel with the ELA scanning direction.

3. Results and discussion

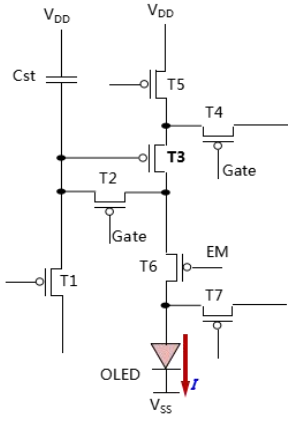

Figure 2. The schematic of conventional 7T1C circuit.

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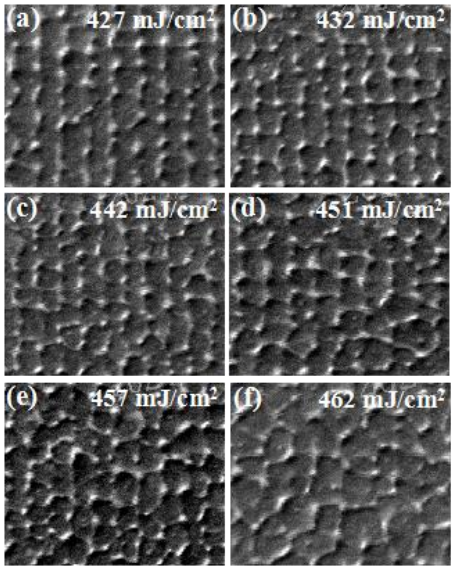

Figure 3. Scanning electron microscope images of poly-Si on glass substrate. Power density of these films was (a) 427 mJ/cm^2, (b) 432 mJ/cm^2, (c) 442 mJ/cm^2, (d) 451 mJ/cm^2, (c) 457 mJ/cm^2, and (d) 462 mJ/cm^2, respectively.

The conventional 7T1C circuit is shown in Fig. 2, and the T3 as driving TFT determines the current passing through the OLED, which directly affects the brightness. On the off-state, the kink effect of T3 will induced bright points. Therefore, it is necessary to study the effect of ELA scan direction on TFT properties.

Scanning electron microscope images of poly-Si are shown in Fig. 3, and the results show that the disorder of grain arrangement increases with the energy density increased. The energy density at 432 mJ/cm^2 was chosen to study the study the effect of orientation on TFT performance due to its regular arrangement.

Fig. 4 shows the AFM image of the ELA poly-Si surface which can be seen that the grains are arranged in a regular pattern and a "line" be formed along the ELA scan direction. The direction along the ELA scan direction be defined as the Y-axis and the direction vertical the ELA scan direction be defined as the X-axis. The nine lines are uniformly taken along the Y-axis and X-axis as shown in Fig. 4, separately. High grain boundaries with high potential barriers that can affect the mobility of charge carriers. Therefore, only grain boundaries with a protrusion height greater than 10 nm were counted as shown in Table 1. It can be seen from from the Table 1, the number of grain boundaries per micrometer along the Y-axis is less than X-axis. The results indicated that the carrier along the Y-axis with lower barrier which cause higher mobility and higher leakage current.

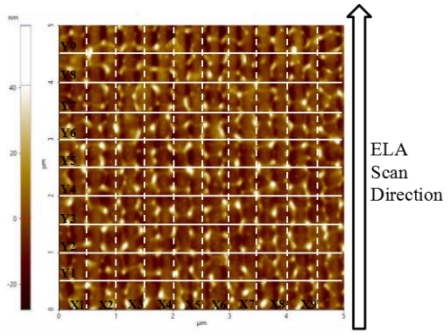

Figure 4. An Atomic force microscopy (AFM) image of the ELA poly-Si surface. The viewing area is 5 × 5 μm^2.

Table 1. Counting the height and number of protrusions along the X and Y axes.

Average height of protrusion (H>10 nm)/nm		Number of grain boundaries per micrometer	
Y-axis	23.34	Y-axis	13.20
X-axis	24.37	X-axis	17.20

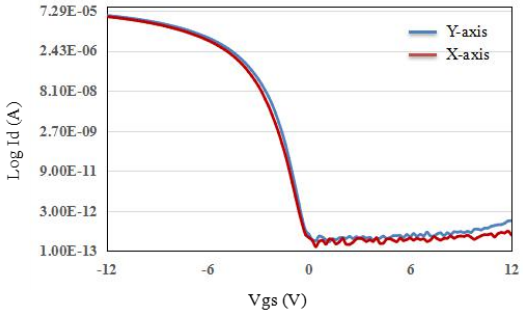

Figure 5. Electrical characteristics of Id-Vg on ID = -5.1V of two different ELA scan direction: red line is X-axis TFT and blue line is Y-axis TFT.

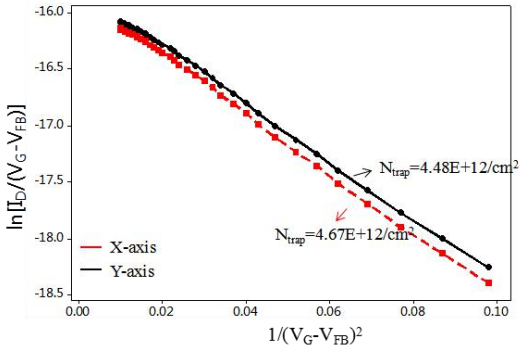

Figure 6. Levinson-Proano plot with low-temperature polycrystalline silicon thin-film transistor (LTPS TFT) on Y-axis TFT and X-axis TFT.

Table 2. Electrical characteristics of two different ELA scan direction with Id= -5.1V

Direction	Y-axis	X-axis
Vth	-1.92	-2.16
Ion	3.42E-05	3.02E-05
Ioff	4.87E-13	2.23E-13
SS	0.38	0.41
DR Range	2.02	2.08
Mobility	66.1	62.99
Nit	9.75E+11	1.07E+12
Ntrap	4.48E+12	4.67E+12

The transfer characteristic curve of the Y-axis TFT and X-axis TFT are shown in Fig. 5. The grain boundary trap-state densities (Ntrap) for both Y-axis and X-axis thin-film transistors (TFTs) employing the Levinson and Proano method [9, 10]. Fig. 6 presents the plots of $\ln[I_D/(V_G - V_{FB})]$ versus $1/(V_G - V_{FB})^2$ at low drain voltage (V_D) and high gate voltage (V_G). The flat-band voltage (V_{FB}) is defined as the gate voltage that minimizes the drain current obtained from the transfer characteristics at $V_D = -0.1$ V. The grain boundary trap-state density was determined by calculating the square root of the slope from Fig. 6 using the relevant equation 1. Additionally, interface trap states at the poly-Si/SiO_2 interface were generated and could be extracted. By disregarding the depletion capacitance in the active layer, the effective interface trap-state density (Nit) could be evaluated from the subthreshold swing (SS).

$$N_{trap} = \frac{C_{ox}}{q}\sqrt{|slope|} \tag{1}$$

$$N_{it} = \frac{C_{ox}}{q}\frac{SS}{2.3kT/q} \quad 1 \tag{2}$$

Table 2 shows the electrical characteristics for two different ELA scanning directions of TFTs. It can be seen from Table 2 that the Y-axis TFT with slightly red-shift Vth, accompanied by a marginally higher Ion, and the SS and DR ranges experience slight decreases due to the higher mobility. Moreover, it showed be noticed that the Ioff of Y-axis TFT higher than X-axis 2.64E-13 which may produced more off-state leakage current type bright points. And it is apparent that the grain boundary trap-state density and the interface trap-state density of X-axis TFT is higher than Y-axis TFT which can explained the differences in electronic characteristics.

The grain boundary barrier of Y-axis TFT and X-axis TFT were calculated by the Arrhenius equation to determine their differences in barrier under same voltage.The grain boundary barrier can extract activation energy from the drain current of the device by the slope of the Arrhenius curve *lnI$_D$ vs. -1/kT*, and the Arrhenius equation [11-12]:

$$k = Ae^{(E_\alpha/RT)} \tag{3}$$

where E_α is the activation energy, A is the pre-exponential factor, R is the gas constant, T indicates the temperature (K), and k is the reaction rate constant.

In poly-crystalline semiconductor, if the carriers within the grains with energy higher than the grain boundary barrier ($E_\alpha > qB$), they can traverse the barrier via hot electron emission to enter adjacent grains, assuming a uniform distribution of grains along the channel direction. The relationship between carrier mobility and barrier B is as follows:

$$\mu_{eff} = \mu_i \exp\frac{-qB}{kT} \tag{4}$$

Where, μ_{eff} is the effective carrier mobility, μ_i is the mobility within the grain, Ψ_B is grain boundary barrier, k is the Boltzmann constant, and T is the absolute temperature. Eq. 4 can be written as:

$$\mu_{eff} = \mu_i \exp(\frac{-E_\alpha}{kT}) \tag{5}$$

For large grain poly-crystalline silicon semiconductor thin film transistors, the formula for the drain current of a TFT with channel length L and width W in the saturation regions is:

$$I_{DS} = \mu_{FE} C_i \frac{W}{2L}(V_{GS} - V_{TH})^2 \tag{6}$$

From Eq. 5 and Eq. 6, the relationship between drain current ID and Eα can be obtained:

$$I_D = B * \exp(\frac{-E_\alpha}{kT}) \tag{7}$$

Eq. 7 can be rearranged as its logarithmic form, as shown in Eq. 6:

$$\ln I_D = \ln B + (\frac{-E_\alpha}{kT}) \tag{8}$$

B is $\mu_i C_i \frac{W}{2L}(V_{GS} - V_{TH})^2$, in which is not related to temperature. By the relationship between *lnID vs. -1/kT*, the activation energy E_a can be determined. In organic light-emitting diode (OLED) panel, the driving TFT in the circuit operates in the saturation region.

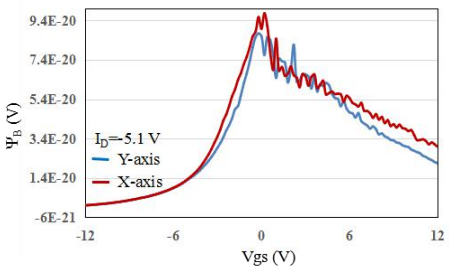

Figure 7. The activation energy of p-type LTPS-TFT in saturated region.

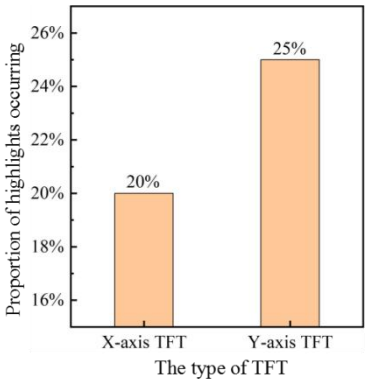

Figure 8. The proportion of bright points occurring on X-axis TFT and Y-axis TFT.

Fig. 7 shows the activation energy of p-type LTPS-TFT in saturated region. For the driving TFT in the circuit operating in the saturation region, the potential barrier decreases with the increase of negative voltage on the on-state as shown in Fig. 7. It is worth noticed that the barrier of Y-axis TFT is lower than that of X-axis TFT resulting in higher carrier mobility, which is consistent with the characteristic results. The potential barrier decreases with increasing voltage on the off-state is caused by the drain-induced barrier lowering (DIBL) [13]. The Y-axis TFT with lower barrier on the off-state and lower trap-state density than X-axis TFT which clarified the Y-axis TFT has larger off-state leakage current. The proportion of bright points occurring on TFT with current along the ELA scan direction (Y-axis TFT) and

vertical the ELA scan direction (X-axis TFT) is shown in Fig. 8. The results give the support for reduce the bright points during the TFT fabricated process.

4. Conclusions

In this paper, two different crystal orientations TFTs were fabricated through ELA to study the effect on characteristics. The TFT with current along the ELA scan direction exhibited higher mobility, and higher Ioff with lower grain boundary trap-state density and lower poly-Si/Si interface trap-state density leading to more off-state leakage current bright points. The AFM results showed that the current along the ELA scan direction will through fewer grain boundary. The activation energy of two types TFT on saturation region is calculated. The results demonstrated that on the off-state the TFT of current along the ELA scan direction with lower barrier which induced higher off-state leakage current. Therefore, the TFT with current along the ELA scan direction on the panel have a higher probability of forming off-state leakage type bright points.

5. References

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